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INTEGRATED MULTIPROTOCOL PROCESSOR (IMP)

DESCRIPTION

The IMP is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard, TS 68000/TS 68008 microprocessor core and a flexible communications architecture. This multichannel communications device may be configured to support a number of popular industry interfaces, including those for the integrated services digital network (ISDN) basic rate and terminal adaptor applications. Through a combination of architectural and programmable features, concurrent operation of different protocols is easily achieved using the IMP. Data concentrators, line cards, bridges, and gateways are examples of suitable applications for this versatile device.
The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of an TS 68000/TS 68008 microprocessor core, a system integration block (SIB), and a communications processor (CP). The TS 68302 block diagram is shown in Figure 1.

MAIN FEATURES

The features of the IMP are as follows :

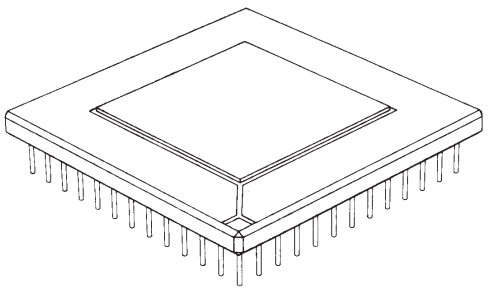
- TS 68000/TS 68008 microprocessor core supporting a 16- or 8-Bit TS 68000 family.
- SIB including :
  - independent direct memory access (IDMA) controller,
  - interrupt controller with two modes of operation,
  - parallel input/output (I/O) ports, some with interrupt capability,
  - on-chip usable 1152 bytes of dual-port random-access memory (RAM),
  - three timers, including a watchdog timer,
  - four programmable chip-select lines with wait-state logic,
  - programmable address mapping of dual-port RAM and IMP registers,
  - on-chip clock generator with an output clock signal,
  - system control : system control register ; bus arbitration logic with low interrupt latency support ; hardware watchdog for monitoring bus activity ; low power (standby) modes ; disable CPU logic (TS 68000) ; freeze control for debugging selected on-chip peripherals ; DRAM refresh controller.
- CP including :
  - main controller (RISC processor),
  - three full-duplex serial communication controllers (SCCs),
  - six serial direct memory access (SDMA) channels dedicated to the three SCCs,
  - flexible physical interface accessible by SCCs for interchip digital link (IDL), general circuit interface (GCI, see note), pulse code modulation (PCM), and nonmultiplexed serial interface (NMSI) operation,
  - serial communication port (SCP) for synchronous communication, clock rate up to 4.096 MHz
  - serial management controllers (SMCs) for IDL and GCI channels.
- Frequency of operation : 16.67 MHz.
- Power supply : 5 V_{DC} ± 10 %.

SCREENING / QUALITY

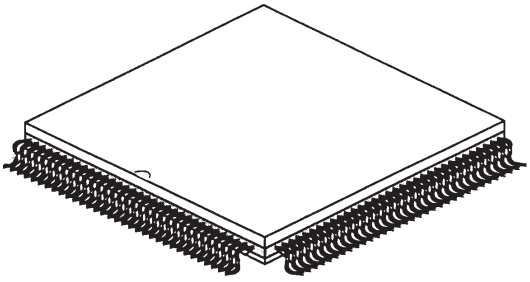
This product is manufactured in full compliance with either :

- MIL-STD-883 (class B).
- DESC. Drawing 5962-93159.
- or according to TCS standards.

Note : GCI is sometimes referred to as IOM2.



R suffix
PGA 132
(Ceramic Pin Grid Array)



A suffix
CERQUAD 132
(Ceramic Quad Flat Pack)

See the ordering information page 37.

Pin connection : see page 4.

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A - GENERAL DESCRIPTION

1 - INTRODUCTION

The TS 68302 integrated multiprotocol processor (IMP) is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard TS 68000 microprocessor core and a flexible communications architecture. The IMP may be configured to support a number of popular industry interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adaptor applications. Concurrent operation of different protocols is easily achieved through a combination of architectural and programmable features. Data concentrators, line cards, bridges, and gateways are examples of suitable applications for this device.

The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of an TS 68000 microprocessor core, a system integration block (SIB), and a communications processor (CP).

Figure 1 is a block diagram of the TS 68302. The processor can be divided into two main sections : the bus controller and the micromachine. This division reflects the autonomy with which the sections operate.

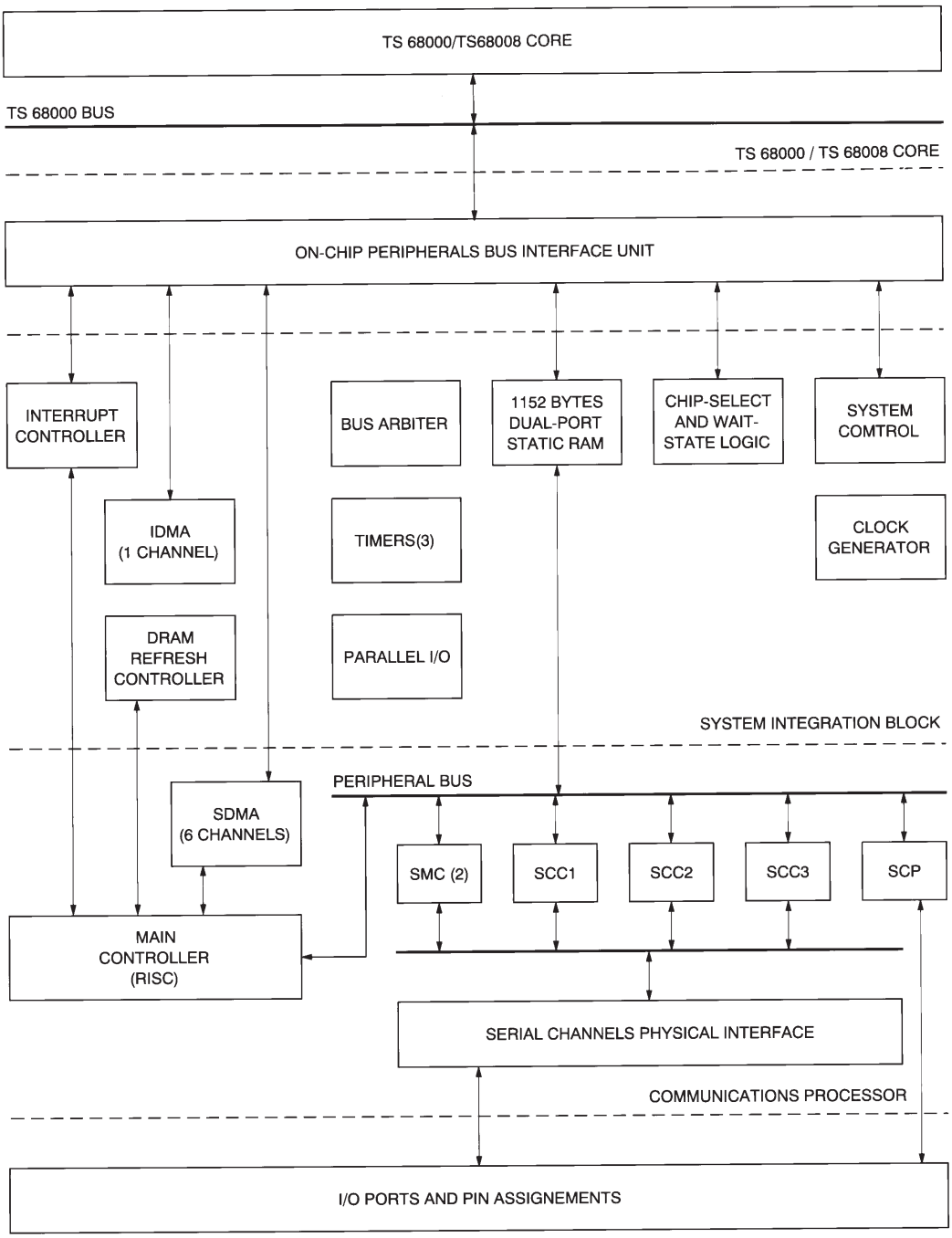


Figure 1 : TS 68302 block diagram.

2 - PIN ASSIGNMENTS

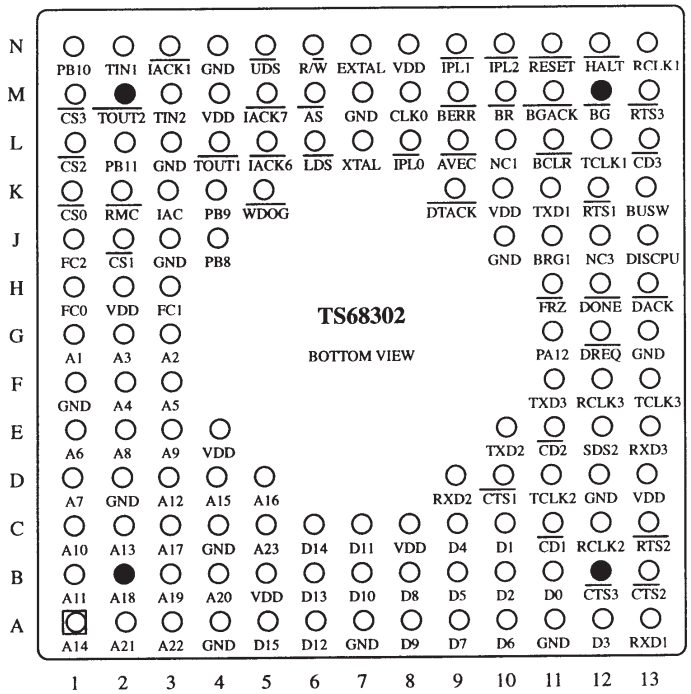

TS68302
BOTTOM VIEW
N PB10 TIN1 IACK1 GND UDS R/W EXTAL VDD IPL1 IPL2 RESET HALT RCLK1
M CS3 TOUT2 TIN2 VDD IACK7 AS GND CLK0 BERR BR BGACK BG RTS3
L CS2 PB11 GND TOUT1 IACK6 LDS XTAL IPL0 AVEC NC1 BCLR TCLK1 CD3
K CS0 RMC IAC PB9 WDOG DTACK VDD TXD1 RTS1 BUSW
J FC2 CS1 GND PB8 GND BRG1 NC3 DISCPU
H FC0 VDD FC1 FRZ DONE DACK
G A1 A3 A2 PA12 DREQ GND
F GND A4 A5 TXD3 RCLK3 TCLK3
E A6 A8 A9 VDD TXD2 CD2 SDS2 RXD3
D A7 GND A12 A15 A16 RXD2 CTS1 TCLK2 GND VDD
C A10 A13 A17 GND A23 D14 D11 VDD D4 D1 CD1 RCLK2 RTS2
B A11 A18 A19 A20 VDD D13 D10 D8 D5 D2 D0 CTS3 CTS2
A A14 A21 A22 GND D15 D12 GND D9 D7 D6 GND D3 RXD1
1 2 3 4 5 6 7 8 9 10 11 12 13

Figure 2.1 : PGA terminal designation.

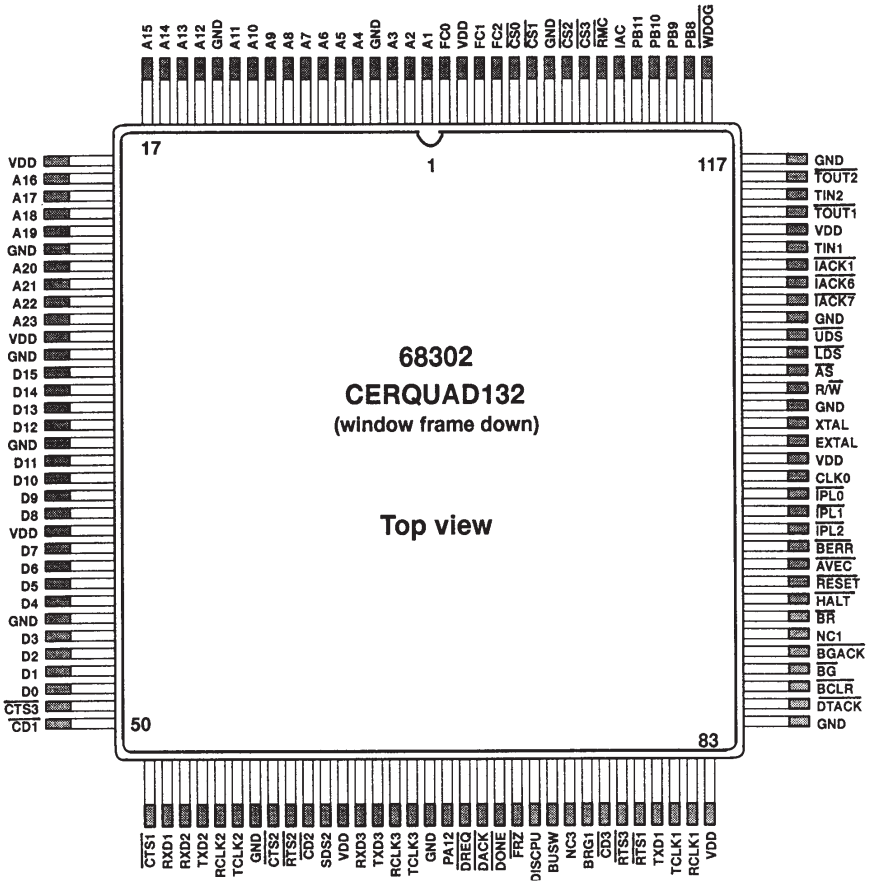

68302
CERQUAD132
(window frame down)
Top view
17
1
117
50
83
A15 A14 A13 A12 GND A11 A10 A9 A8 A7 A6 A5 A4 GND A3 A2 A1 FC0 VDD FC1 FC2 CS0 CS1 GND CS2 CS3 RMC IAC PB11 PB10 PB9 PB8 WDOG
VDD A16 A17 A18 A19 GND A20 A21 A22 A23 VDD GND D15 D14 D13 D12 GND D11 D10 D9 D8 VDD D7 D6 D5 D4 GND D3 D2 D1 D0 CTS3 CD1
GND TOUT2 TIN2 TOUT1 VDD TIN1 IACK1 IACK6 IACK7 GND UDS LDS AS R/W GND XTAL EXTAL VDD CLK0 IPL0 IPL1 IPL2 BERR AVEC RESET HALT BR NC1 BGACK BG BCLR DTACK GND
CTS1 RXD1 RXD2 TXD2 RCLK2 TCLK2 GND CTS2 RTS2 CD2 SDS2 VDD RXD3 TXD3 RCLK3 TCLK3 GND PA12 DREQ DACK DONE FRZ DISCPU BUSW NC3 BRG1 CD3 RTS3 RTS1 TXD1 TCLK1 RCLK1 VDD

Figure 2.2 : CERQUAD terminal designation.

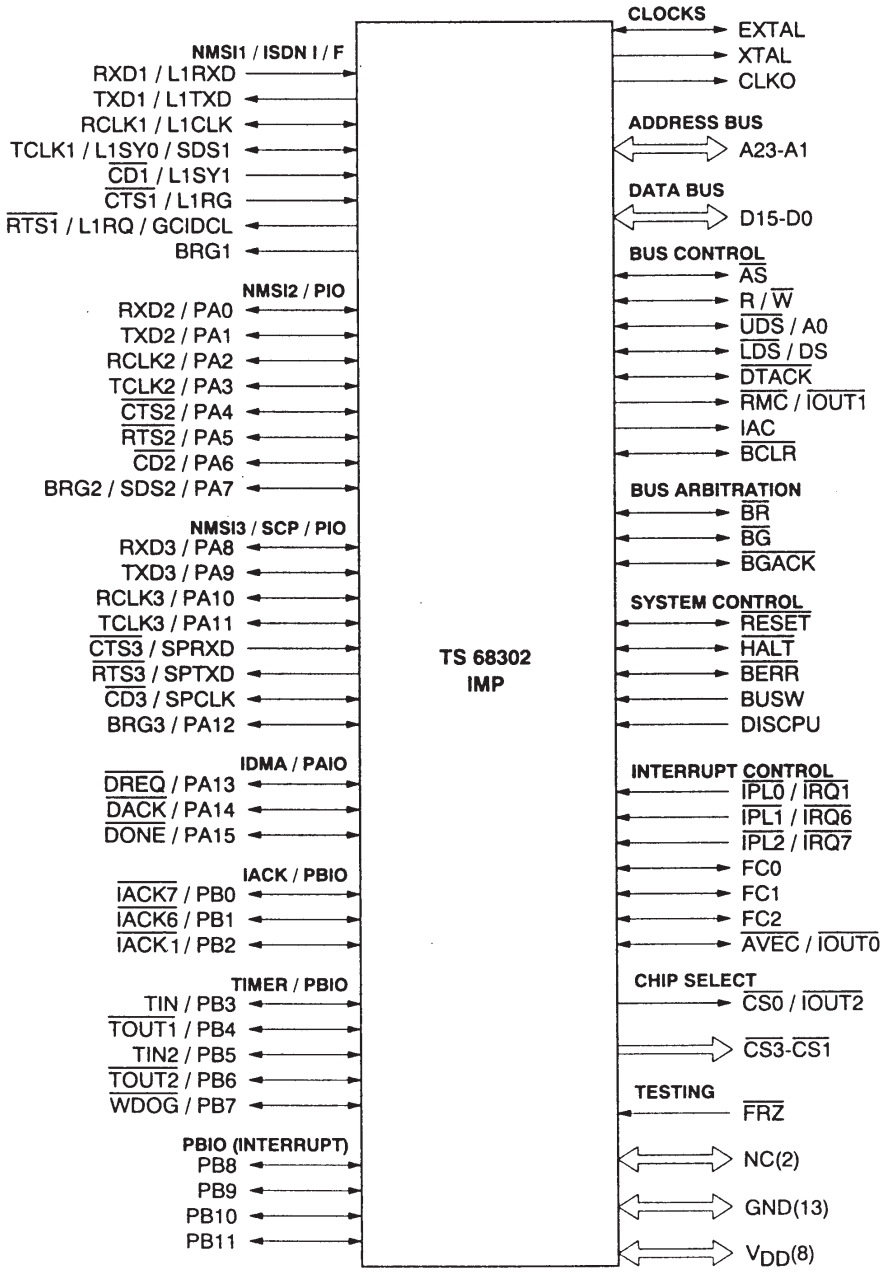


Figure 3 : Functional signal groups.

3 - SIGNAL DESCRIPTIONS

The input and output signals of the TS 68302 are organized into functional groups as shown in Table 1. Refer to TS 68302 Integrated Multiprotocol Processor User's Manual, for detailed information on the TS 68302 signals.

Table 1 - Signal definitions

Functional group	Signals	Num.
Clocks	XTAL, EXTAL, CLKO	3
System Control	$\overline{\text{RESET}}$, $\overline{\text{HALT}}$, $\overline{\text{BERR}}$, BUSW, DISCPU	5
Address Bus	A23-A1	23
Data Bus	D15-D0	16
Bus Control	$\overline{\text{AS}}$, R/$\overline{\text{W}}$, $\overline{\text{UDS}}$/A0, $\overline{\text{LDS}}$/$\overline{\text{DS}}$, $\overline{\text{DTACK}}$	5
Bus Control	$\overline{\text{RMC}}$, IAC, $\overline{\text{BCLR}}$	3
Bus Arbitration	$\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{BGACK}}$	3
Interrupt Control	$\overline{\text{IPL2}}$-$\overline{\text{IPL0}}$, FC2-FC0, $\overline{\text{AVEC}}$	7
NMSI1/ISDN I/F	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, BRG1	8
NMSI2/PIO	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, SDS2	8
NMSI3/SCP/PIO	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, PA12	8
IDMA/PAIO	$\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, $\overline{\text{DONE}}$	3
IACK/PBIO	$\overline{\text{IACK7}}$, $\overline{\text{IACK6}}$, $\overline{\text{IACK1}}$	3
Timer/PBIO	TIN2, TIN1, $\overline{\text{TOUT2}}$, $\overline{\text{TOUT1}}$, $\overline{\text{WDOG}}$	5
PBIO	PB11-PB8	4
Chip Select	$\overline{\text{CS3}}$-$\overline{\text{CS0}}$	4
Testing	$\overline{\text{FRZ}}$ (2 Spare)	3
V_{DD}		8
GND		13

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the processor TS 68302, 16.67 MHz, in compliance either with MIL-STD-883 class B or with TCS standards.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-M-38535 : general specifications for microcircuits.
3) Desc Drawing : 5962-93159 (planned).

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2.1 and 2.2.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-M-38535.

3.2.3 · Package

The macrocircuits are packaged in hermetically sealed ceramic packages which is conform to case outlines of MIL-M-38535 appendix A (when defined) :

- 132-pin Ceramic Pin Grid Array (PGA),
- 132-pin Ceramic Quad Flat Pack (CERQUAD).

The precise case outlines are described on Figures 2.1 and 2.2.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (see Table 2)

Table 2

Symbol	Parameter	Min	Max	Unit
P_D	Power dissipation (typical at 16.67 MHz) - Note 1	53	64	mA
P_D	Power dissipation (typical at 8 MHz) - Note 1	26	31	mA
LP_D	Low power mode dissipation (typical at 16.67 MHz) - Note 2		36	mA
LP_D	Lowest power mode dissipation (typical at 16.67 MHz) - Note 3		32	mA
LP_D	Lowest power mode dissipation (typical at 50 kHz) - Note 4		1	mA

Note 1 : The values shown are typical. The typical value varies as shown, based on how many IMP on-chip peripherals are enabled and the rate at which they are clocked.

Note 2 : LPREC = 0. Divider = 2.

Note 3 : LPREC = 1. Divider = 1024.

Note 4 : The stated frequency must be externally applied to EXTAL only after the IMP has been placed in the lowest power mode with LPREC = 1. The 68000 core is not specified to operate at this frequency, but the rest of the IMP is. In this configuration, the user does not divide the clock internally using the LPCD4-LPCD0 bits in the system control register.

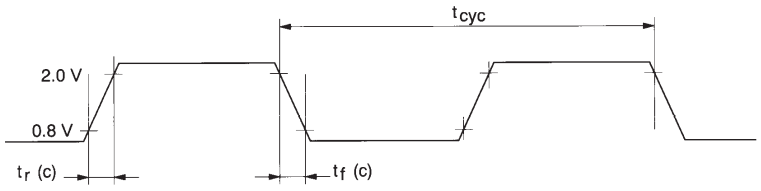
3.3.2 · Recommended condition of use

Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

Table 3

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IL}	Low level input voltage	− 0.3	+ 0.5	V
V_{IH}	High level input voltage	2.4	5.5	V
T_{case}	Operating temperature	− 55	+ 125	°C
$t_r(c)$	Clock rise time - see Figure 4		5	ns
$t_f(c)$	Clock fall time resistance - see Figure 4		5	ns
f_c	Clock frequency - see Figure 4	8	16.67	MHz
t_{cyc}	Cycle time - see Figure 4	60	125	ns

This device contains protective circuitry to protect the inputs against damage due to high static voltages or electrical fields ; however, it is advises that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 4 : Clock input timing diagram.

3.4 · Thermal characteristics (at 25°C)

Table 4

Package	Symbol	Parameter	Value	Unit
PGA 132	θJA	Thermal resistance - ceramic junction to ambient	33	°C/W
	θJC	Thermal resistance - ceramic junction to case	5	°C/W
CERQUAD 132	θJA	Thermal resistance - ceramic junction to ambient	46	°C/W
	θJC	Thermal resistance - ceramic junction to case	2	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output pins — user determined

Note : For $T_A = 70°C$ and $P_D = 0.5$ W @ 12.5 MHz $T_j = 88°C$.

For most applications $P_{I/O} < 0{,}30\ P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θJ_C. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or TCS standards.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

3.6.1 - Thomson logo

3.6.2 - Manufacturer's part number

3.6.3 - Class B identification

3.6.4 - Date-code of inspection lot

3.6.5 - ESD identifier if available

3.6.6 - Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified. For inspection purpose, refer to relevant specification :

– DESC see § 4.1

Tables 5-6 : Static electrical characteristics for all electrical variants. Test methods refer to IEC 748-2 method number, where existing. See § 5.2.

Tables 7-8 : Dynamic electrical characteristics. Test methods refer to § 5.3 of this specification.

Table 5 - DC electrical characteristics

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55°C / +125°C or −40°C / +85°C

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage (except EXTAL)	2.0	V_{DD}	V
V_{IL}	Input low voltage (except EXTAL)	V_{SS} −0.3	0.8	V
V_{CIH}	Input high voltage (EXTAL)	4.0	V_{DD}	V
V_{CIL}	Input low voltage (EXTAL)	V_{SS} −0.3	0.6	V
I_{IN}	Input leakage current		20	µA
C_{IN}	Input capacitance all pins		15	pF
I_{TSI}	Three-state leakage current (2.4 V / 0.5 V)		20	µA
I_{OD}	Open drain leakage current (2.4 V)		20	µA
V_{OH}	Output high voltage (I_{OH} = 400 µA)	V_{DD} −1.0		V

Table 5 - DC electrical characteristics (continued)

V_{CC} = 5.0 V_{dc} ±10 % ; GND = 0 V_{dc} ; T_C = −55°C / +125°C or −40°C / +85°C

Symbol	Parameter	Min	Max	Unit
V_{OL}	Output low voltage			
	(I_{OL} = 3.2 mA) A1-A23, PB0-PB11, FC0-FC3, $\overline{CS0}$-$\overline{CS3}$ IAC, $\overline{AVEC}$, BG, RCLK1, $\overline{RCLK2}$, $\overline{RCLK3}$, TCLK1, TCLK2, TCLK3, $\overline{RTS1}$, $\overline{RTS2}$, $\overline{RTS3}$, $\overline{SDS2}$, PA12, RXD2, RXD3, $\overline{CTS2}$, $\overline{CD2}$, $\overline{CD3}$, $\overline{DREQ}$		0.5	V
	(I_{OL} = 5.3 mA) $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{BERR}$, $\overline{BGACK}$, $\overline{BCLR}$, $\overline{DTACK}$, $\overline{DACK}$, $\overline{RMC}$, $\overline{RMC}$, DO-D15, $\overline{RESET}$		0.5	V
	(I_{OL} = 7.0 mA) TXD1, TXD2, TXD3		0.5	V
	(I_{OL} = 8.9 mA) $\overline{BR}$, $\overline{DONE}$, $\overline{HALT}$, ($\overline{BR}$ as output)		0.5	V
	(I_{OL} = 3.2 mA) CLKO		0.4	V
O_{CLK}	Output drive CLKO		50	pF
O_{GCI}	Output drive ISDN I/F (GCI mode)		150	pF
O_{ALL}	Output drive All other pins		130	pF

Table 6 - DC electrical characteristics - NMSI1 in IDL mode

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	Power		4.5	5.0	5.5	V
V_{SS}	Common		0	0	0	V
T	Temperature	Operating range	−55	25	+125	°C
Input pin characteristics : L1CLK, L1SY1, L1RXD, L1GR						
V_{IL}	Input low level voltage	(% of V_{DD})	−10 %		+20 %	V
V_{IH}	Input high level voltage		V_{DD} −20 %		V_{DD} +10 %	V
I_{IH}	Input low level current	V_{in} = V_{SS}			± 10	µA
I_{IH}	Input high level current	V_{in} = V_{DD}			± 10	µA
Output pin characteristics : L1TXD, SDS1-SDS2, L1RQ						
V_{OL}	Output low level voltage	I_{OL} = 2.0 mA	0		0.50	V
V_{OH}	Output high level voltage	I_{OH} = 2.0 mA	V_{DD} −0.5		V_{DD}	V

5.3 - Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range −55°C to +125°C or −40°C to +85°C depending on selection see § 11 and V_{CC} in the range 4.5 V to 5.5 V V_{IL} = 0.5 V and V_{IH} = 2.4 V.

The INTERVAL numbers (NUM) refer to the timing diagrams. See Figures 5 to 25.

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock (CLKO pin) and possibly to one or more other signals.

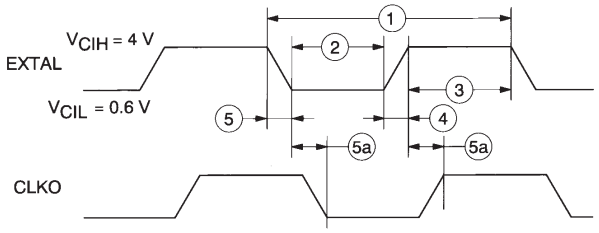


Figure 5 : Clock timing diagram.

Table 7 - AC electrical specifications - Clock timing (see Figure 6)

Num.	Symbol	Parameter	Min	Max	Unit
	f	Frequency of operation	8	16.67	MHz
1	t_{cyc}	Clock period (EXTAL)	60	125	ns
2, 3	t_{CL}, t_{CH}	Clock pulse width (EXTAL)	25	62.5	ns
4, 5	t_{Cr}, t_{Cf}	Clock rise and fall times (EXTAL)		5	ns
5a	t_{CD}	EXTAL to CKLO delay - Notes 1 and 2	2	11	ns

Note 1 : CLKO loading is 50 pF max.

Note 2 : CLKO skew from the rising and falling edges of EXTAL will not differ from each other more than 1 ns, if the EXTAL rise time equals the EXTAL fall time.

Table 8 - AC electrical specifications - IMP bus master cycles (see Figures 6, 7 and 8) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
6	$t_{CHFCADV}$	Clock high to FC, address valid		45	ns
7	t_{CHADZ}	Clock high to address, data bus high impedance (maximum)		50	ns
8	t_{CHAFI}	Clock high to address, FC invalid (minimum)	0		ns
9	t_{CHSL}	Clock high to $\overline{AS}$, $\overline{DS}$ asserted - Note 1	3	30	ns
11	t_{AFCVSL}	Address, FC valid to $\overline{AS}$, $\overline{DS}$ asserted (read) / $\overline{AS}$ asserted (write) Note 2	15		ns
12	t_{CLSH}	Clock low to $\overline{AS}$, $\overline{DS}$ negated - Note 1		30	ns
13	t_{SHAFI}	$\overline{AS}$, $\overline{DS}$ negated to address, FC invalid - Note 2	15		ns
14	t_{SL}	$\overline{AS}$ (and $\overline{DS}$ read) width asserted - Note 2	120		ns
14A	t_{DSL}	$\overline{DS}$ width asserted, write - Note 2	60		ns
15	t_{SH}	$\overline{AS}$, $\overline{DS}$ width negated - Note 2	60		ns
16	t_{CHCZ}	Clock high to control bus high impedance		50	ns
17	t_{SHRH}	$\overline{AS}$, $\overline{DS}$ negated to R/$\overline{W}$ invalid - Note 2	15		ns
18	t_{CHRH}	Clock high to R/$\overline{W}$ high - Note 1		30	ns
20	t_{CHRL}	Clock high to R/$\overline{W}$ low - Note 1		30	ns
20A	t_{ASRV}	$\overline{AS}$ asserted to R/$\overline{W}$ low (write) - Notes 2 and 3		10	ns
21	t_{AFCVRL}	Address FC valid to R/$\overline{W}$ low (write) - Note 2	15		ns
22	t_{RLSL}	R/$\overline{W}$ low to $\overline{DS}$ asserted (write) - Note 2	30		ns
23	t_{CLDO}	Clock low to data-out valid		30	ns
25	t_{SHDOI}	$\overline{AS}$, $\overline{DS}$, negated to data-out invalid (write) - Note 2	15		ns
26	t_{DOSL}	Data-out valid to $\overline{DS}$ asserted (write) - Note 2	15		ns
27	t_{DICL}	Data-in valid to clock low (Setup time on read) - Note 4	7		ns
28	t_{SHDAH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{DTACK}$ negated (asynchronous hold) - Note 2	0	110	ns
29	t_{SHDII}	$\overline{AS}$, $\overline{DS}$ negated to data-in invalid (hold time on read)	0		ns
30	t_{SHBEH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{BEER}$ negated	0		ns

Table 8 - AC electrical specifications - IMP bus master cycles (continued) (see Figures 6, 7 and 8) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
31	t_{DALDI}	$\overline{DTACK}$ asserted to data-in valid (setup time) - Notes 2 and 4		50	ns
32	t_{RHr}, t_{RHf}	$\overline{HALT}$ and $\overline{RESET}$ input transition time		150	ns
33	t_{CHGL}	Clock high to $\overline{BG}$ asserted		30	ns
34	t_{CHGH}	Clock high to $\overline{BG}$ negated		30	ns
35	t_{BRLGL}	$\overline{BR}$ asserted to $\overline{BG}$ asserted	2.5	4.5	clks
36	t_{BRHGH}	$\overline{BR}$ negated to $\overline{BG}$ negated - Note 5	1.5	2.5	clks
37	t_{GALGH}	$\overline{BGACK}$ asserted to $\overline{BG}$ negated	2.5	4.5	clks
37A	t_{GALBRH}	$\overline{BGACK}$ asserted to $\overline{BR}$ negated - Note 6	10	1.5	ns/clks
38	t_{GLZ}	$\overline{BG}$ asserted to control, address, data bus high impedance ($\overline{AS}$ negated)		50	ns
39	t_{GH}	$\overline{BG}$ width negated	1.5		clks
44	t_{SHVPH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{AVEC}$ negated	0	50	ns
46	t_{GAL}	$\overline{BGACK}$ width low	1.5		clks
47	t_{ASI}	Asynchronous input setup time - Note 4	10		ns
48	t_{BELDAL}	$\overline{BERR}$ asserted to $\overline{DTACK}$ asserted - Notes 2 and 7	10		ns
53	t_{CHDOI}	Data-out hold from clock high	0		ns
55	t_{RLDBD}	R/$\overline{W}$ asserted to data bus impedance change	0		ns
56	t_{HRPW}	$\overline{HALT}$/$\overline{RESET}$ pulse width - Note 8	10		clks
57	t_{GASD}	$\overline{BGACK}$ negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ driven	1.5		clks
57A	t_{GAFD}	$\overline{BGACK}$ negated to FC	1		clks
58	t_{RHSD}	$\overline{BR}$ negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ driven - Note 5	1.5		clks
58A	t_{RHFD}	$\overline{BR}$ negated to FC - Note 5	1		clks
60	t_{CHBCL}	Clock high to $\overline{BCLR}$ asserted		30	ns
61	t_{CHBCH}	Clock high to $\overline{BCLR}$ negated - Note 9		30	ns
62	t_{CLRML}	Clock low (S0 falling edge during read) to $\overline{RMC}$ asserted		30	ns
63	t_{CHRMH}	Clock high (S7 rising edge during write) to $\overline{RMC}$ negated		30	ns
64	t_{RMHGL}	$\overline{RMC}$ negated to $\overline{BG}$ asserted - Note 10		30	ns

Note 1 : For loading capacitance of less than or equal to 50 pF, subtract 4 ns from the value given in the maximum columns.

Note 2 : Actual value depends on clock period.

Note 3 : When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (± 20 %), subtract 5 ns from the values given in these columns.

Note 4 : If the asynchronous input setup (# 47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$ asserted to data setup time (# 31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (# 27) for the following clock cycle.

Note 5 : The TS 68302 will negate $\overline{BG}$ and begin driving the bus if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.

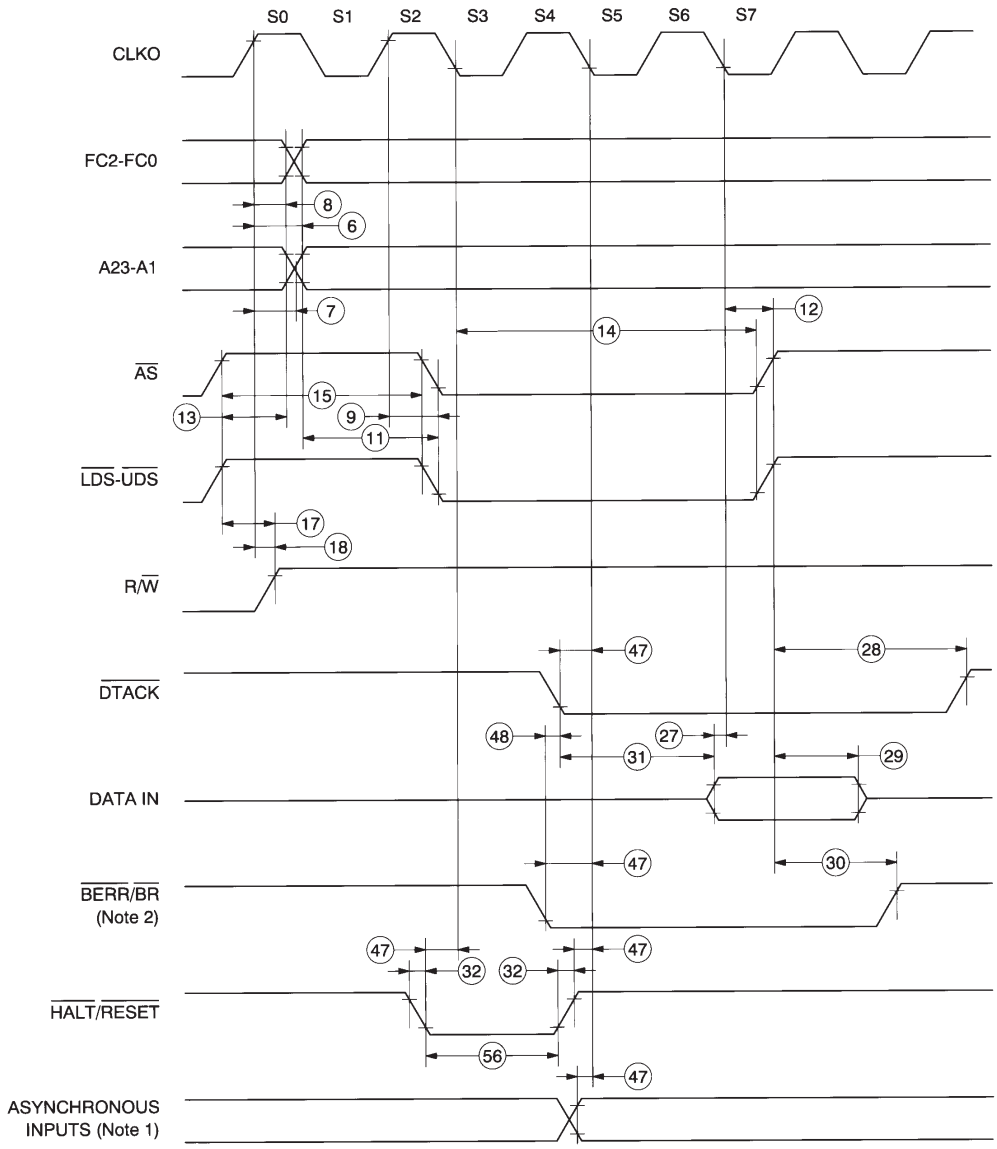
Note 6 : The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, BG may be reasserted.

Note 7 : If # 47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, # 48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is a synchronous input using the asynchronous input setup time (# 47).

Note 8 : For power-up, the TS 68302 must be held in the reset state for 100 ms to allow stabilization of on-chip circuit. After the system is powered up # 56 refers to the minimum pulse width required to reset the processor.

Note 9 : Occurs on S0 of SDMA read/write access when the SDMA becomes bus master.

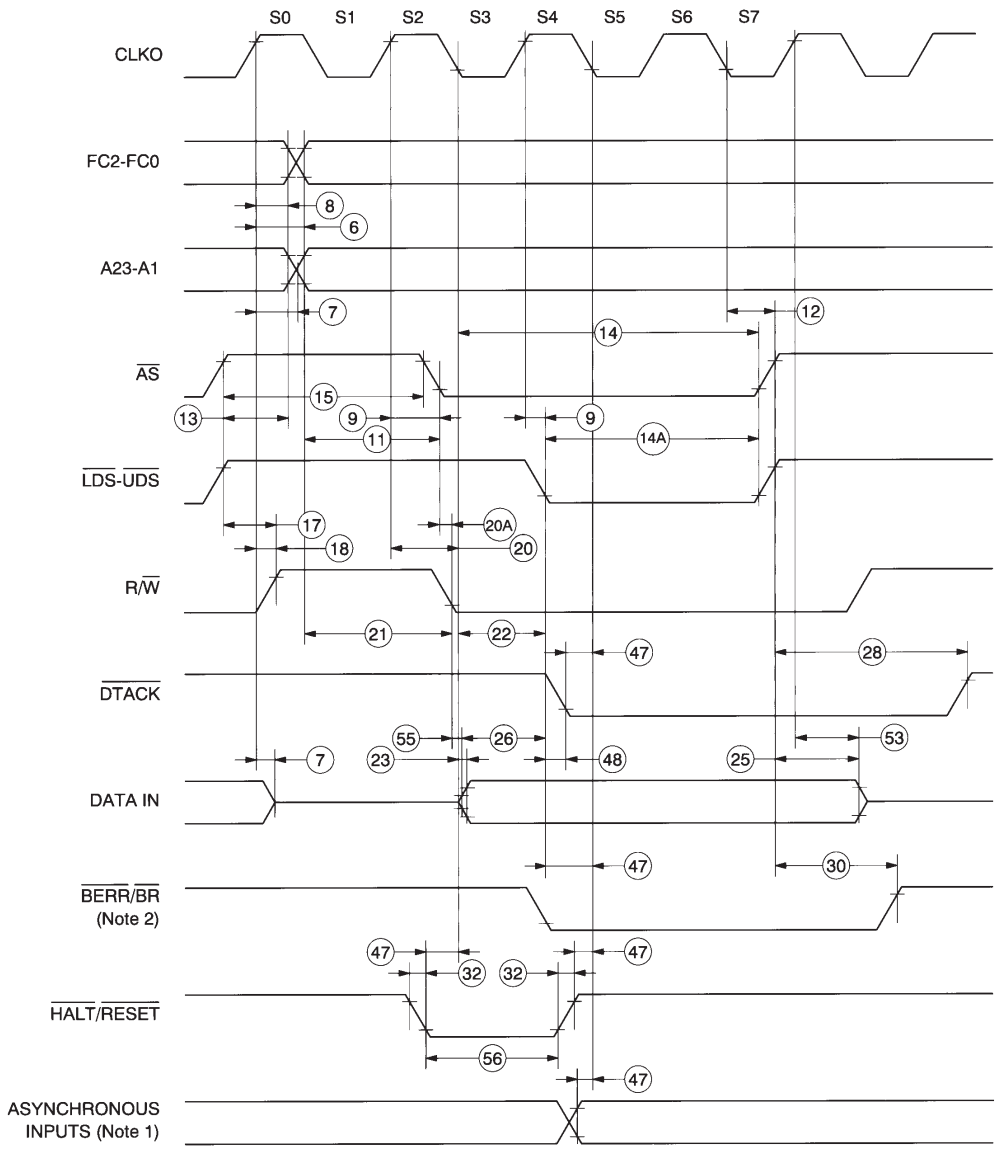
Note 10 : This specification is valid only when the RMCST bit is set in the SCR register.



Notes :

1. Setup time for asymchronous inputs $\overline{IPL2}$-$\overline{IPL0}$ guarantees their recognition at the next falling edge of the clock
2. BR need fall at this time only to ensure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

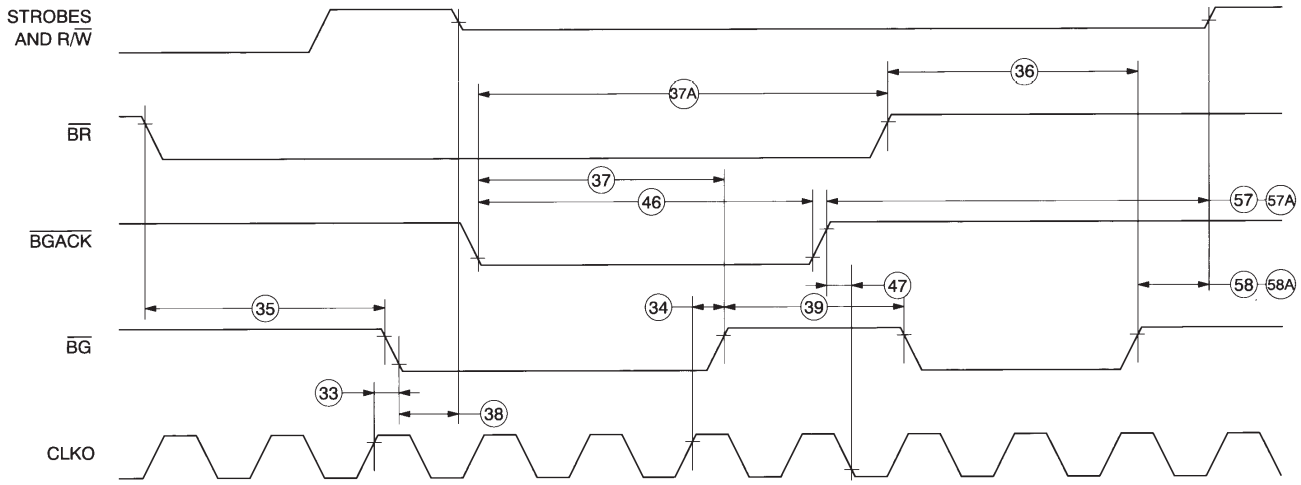
Figure 6 : Read cycle timing diagram.



Notes :

1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (specification #20A)

Figure 7 : Write cycle timing diagram.



Notes : Setup time to the clock (#47) for the asynchronous inputs BERR, BGACK, BR, DTACK, and IPL2-IPL0 guarantees their recognition at the next falling edge of the clock.

Figure 8 : Bus arbitration timing diagram.

Table 9 - AC electrical specifications - DMA (see Figure 9) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
80	t_{REQASI}	DREQ asynchronous setup time - Note 1	15		ns
81	t_{REQL}	DREQ width low - Note 2	2		clk
82	$t_{REQLBRL}$	DREQ low to BR low - Notes 3 and 4		2	clk
83	t_{CHBRL}	Clock high to BR low - Notes 3 and 4		30	ns
84	t_{CHBRZ}	Clock high to BR high impedance - Notes 3 and 4		30	ns
85	t_{BKLBRZ}	BGACK low to BR high impedance - Notes 3 and 4	30		ns
86	t_{CHBKL}	Clock high to BGACK low		30	ns
87	t_{ABHBKL}	AS and BGACK high (the latest one) to BGACK low (when BG is asserted)	1.5	2.5 +30	clk ns
88	t_{BGLBKL}	BG low to BGACK low (no other bus master) Notes 3 and 4	1.5	2.5 +30	clk ns
89	t_{BRHBGH}	BR high impedance to BG high - Notes 3 and 4	0		ns
90	$t_{CLBKLAL}$	Clock on which BGACK low to clock on which AS low	2	2	clk
91	t_{CHBKH}	Clock high to BGACK high		30	ns
92	t_{CLBKZ}	Clock low to BGACK high impedance		15	ns
93	t_{CHACKL}	Clock high to DACK low		30	ns
94	t_{CLACKH}	Clock high to DACK high		30	ns
95	t_{CHDNL}	Clock high to DONE low (output)		30	ns
96	t_{CLDNZ}	Clock low to DONE high impedance		30	ns
97	t_{DNLTCH}	DONE input low to clock high (asynchronous setup)	15		ns

Note 1 : DREQ is sampled on the falling edge of CLK in cycle steal and burst modes.
Note 2 : If # 80 is satified for DREQ, # 81 may be ignored.
Note 3 : BR will not be asserted while AS, HALT, or BERR is asserted.
Note 4 : Specifications are for DISABLE CPU mode only.

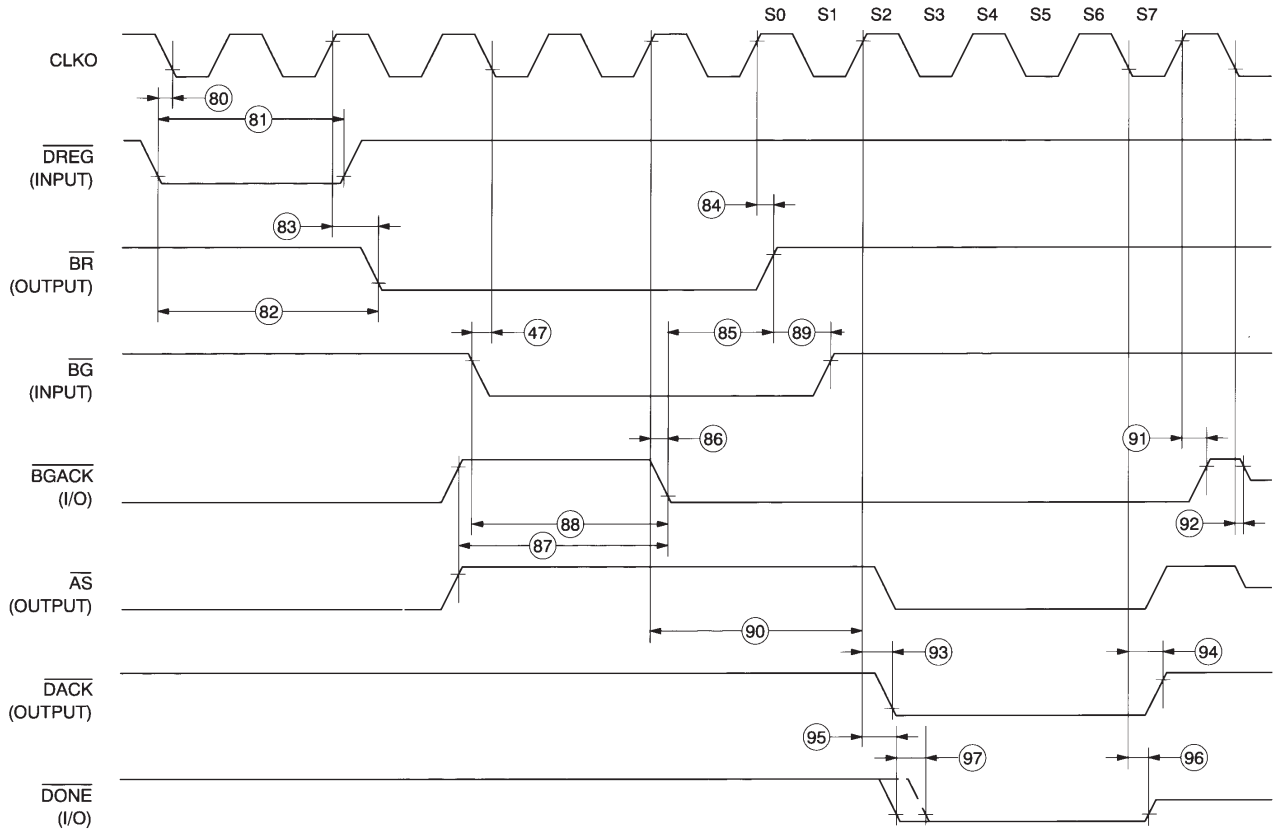


Figure 9 : DMA timing diagram.

Table 10 - AC electrical specifications - External master internal asynchronous read/write cycles (see Figures 10 and 11)
f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
100	t_{RWVDSL}	R/$\overline{W}$ valid to $\overline{DS}$ low	0		ns
101	t_{DSLDIV}	$\overline{DS}$ low to data in valid		30	ns
102	t_{DKLDH}	$\overline{DTACK}$ low to data in hold time	0		ns
103	t_{ASVDSL}	$\overline{AS}$ valid to $\overline{DS}$ low	0		ns
104	t_{DKLDSH}	$\overline{DTACK}$ low to $\overline{DS}$ high	0		ns
105	t_{DSHDKH}	$\overline{DS}$ high to $\overline{DTACK}$ high		45	ns
106	t_{DSIASI}	$\overline{DS}$ inactive to $\overline{AS}$ inactive	0		ns
107	t_{DSHRWH}	$\overline{DS}$ high to R/$\overline{W}$ high	0		ns
108	t_{DSHDZ}	$\overline{DS}$ high to data high impedance		45	ns
108A	t_{DSHDH}	$\overline{DS}$ high to data out hold time	0		ns
109	t_{DSHDOH}	$\overline{DS}$ high to data in hold time - see Note	0		ns
109A	t_{DOVDKL}	Data out valid to $\overline{DTACK}$ low	15		ns

Note : If $\overline{AS}$ is negated before $\overline{DS}$, the data bus could be three-stated (spec 126) before $\overline{DS}$ is negated.

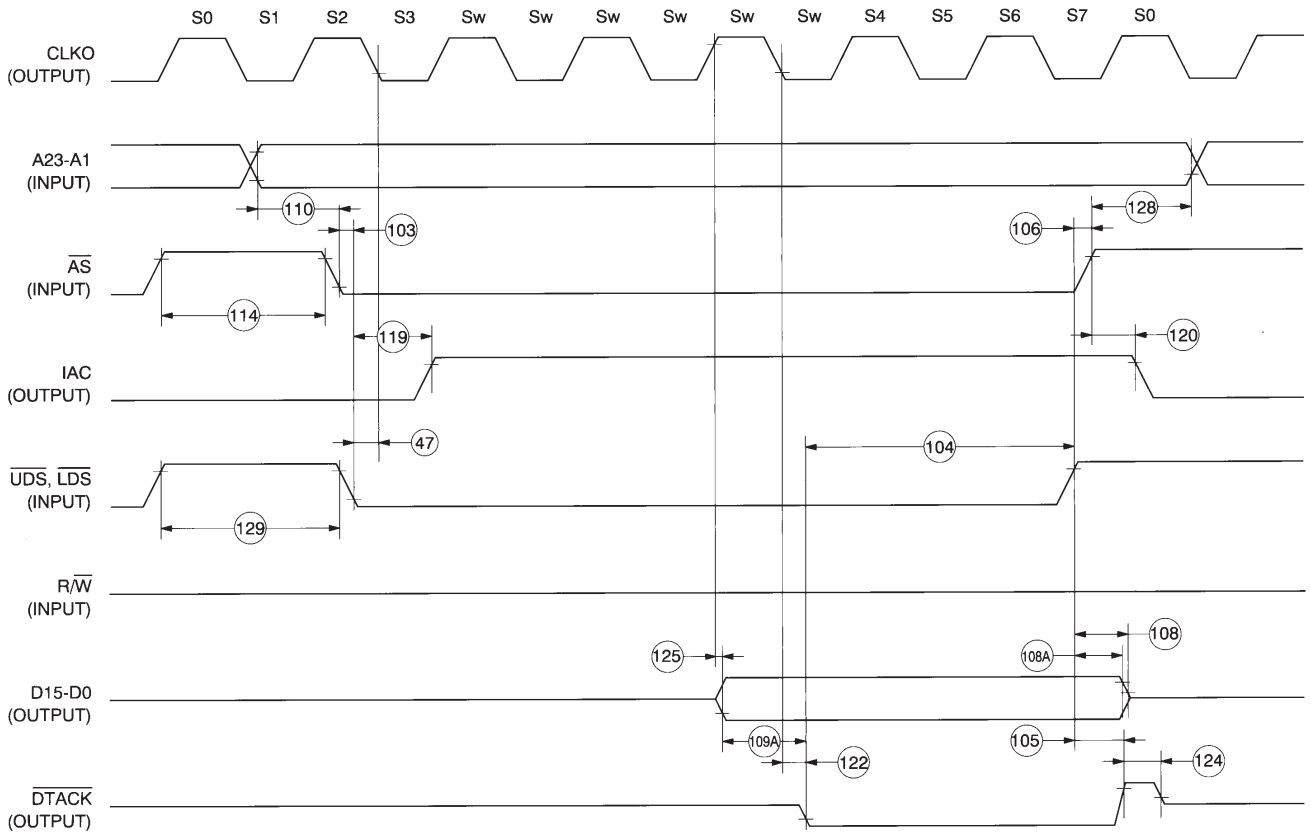


Figure 10 : External master internal asynchronous read cycle timing diagram.

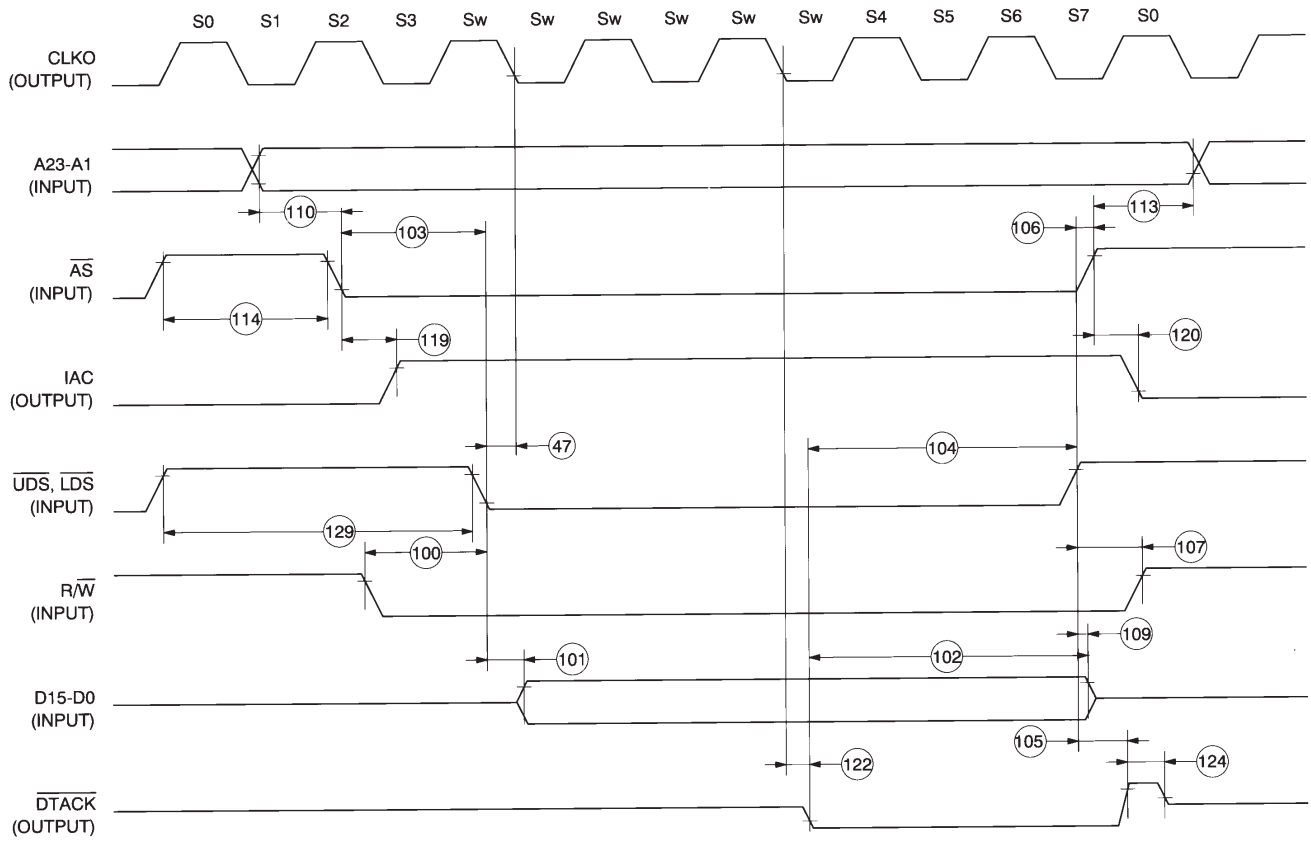


Figure 11 : External master internal asynchronous write cycle timing diagram.

Table 11 - AC electrical specifications - External master internal synchronous read/write cycles
(see Figures 12, 13 and 14) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
110	t_{AVASL}	Address valid to $\overline{AS}$ low	15		ns
111	t_{ASLCH}	$\overline{AS}$ low to clock high	30		ns
112	t_{CLASH}	Clock low to $\overline{AS}$ high		45	ns
113	t_{ASHAH}	$\overline{AS}$ high to adress hold time on write	0		ns
114	t_{ASH}	$\overline{AS}$ inactive time	1		clk
115	t_{SLCH}	$\overline{UDS}$/$\overline{LDS}$ low to clock high	40		ns
116	t_{CLSH}	Clock low to $\overline{UDS}$/$\overline{LDS}$ high		45	ns
117	t_{RWVCH}	R/$\overline{W}$ valid to clock high	30		ns
118	t_{CHRWH}	Clock high to R/$\overline{W}$ high		45	ns
119	t_{ASLIAH}	$\overline{AS}$ low to IAC high		40	ns
120	t_{ASHIAL}	$\overline{AS}$ high to IAC low		40	ns
121	t_{ASLDTL}	$\overline{AS}$ low to $\overline{DTACK}$ low (0 wait state)		45	ns
122	t_{CLDTL}	Clock low to $\overline{DTACK}$ low (1 wait state)		30	ns
123	t_{ASHDTH}	$\overline{AS}$ high to $\overline{DTACK}$ high		45	ns
124	t_{DTHDTZ}	$\overline{DTACK}$ high to $\overline{DTACK}$ high impedance		15	ns
125	t_{CHDOV}	Clock high to data out valid		30	ns
126	t_{ASHDZ}	$\overline{AS}$ high to data high impedance		45	ns
127	t_{ASHDOI}	$\overline{AS}$ high to data out hold time	0		ns
128	t_{ASHAI}	$\overline{AS}$ high to address hold time on read	0		ns
129	t_{SH}	$\overline{UDS}$/$\overline{LDS}$ inactive time	1		clk
130	t_{CLDIV}	Data in valid to clock low	30		ns
131	t_{CLDIH}	Clock low to data in hold time	15		ns

Note : Specifications are valid only when SAM = 1 in the SCR.

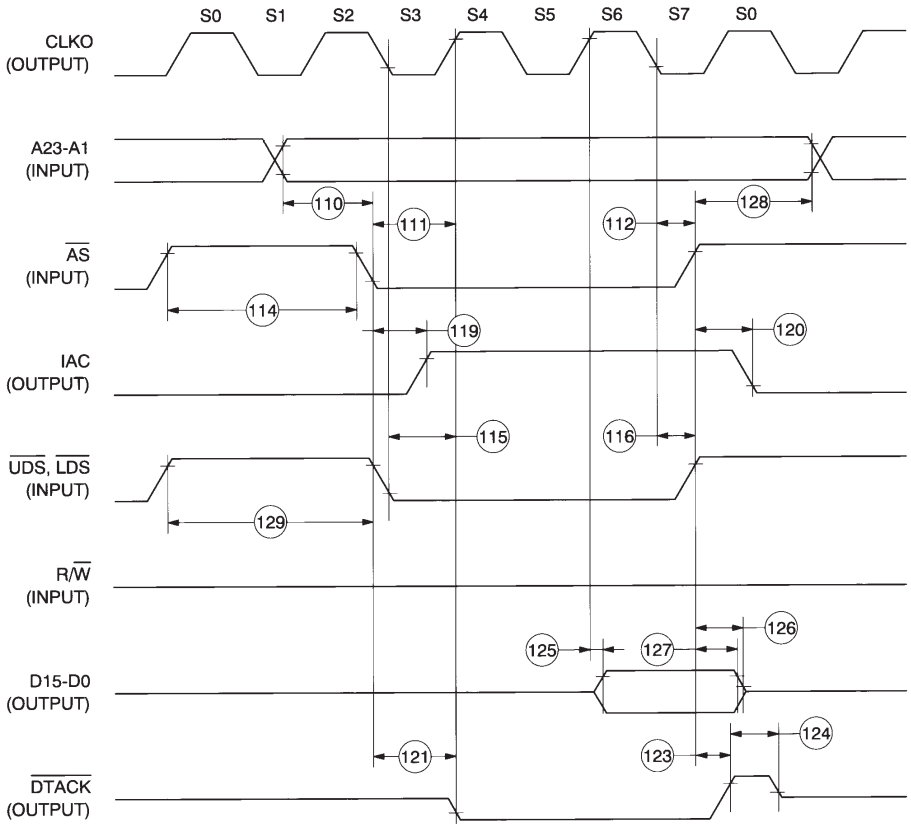


Figure 12 : External master internal synchronous read cycle timing diagram.

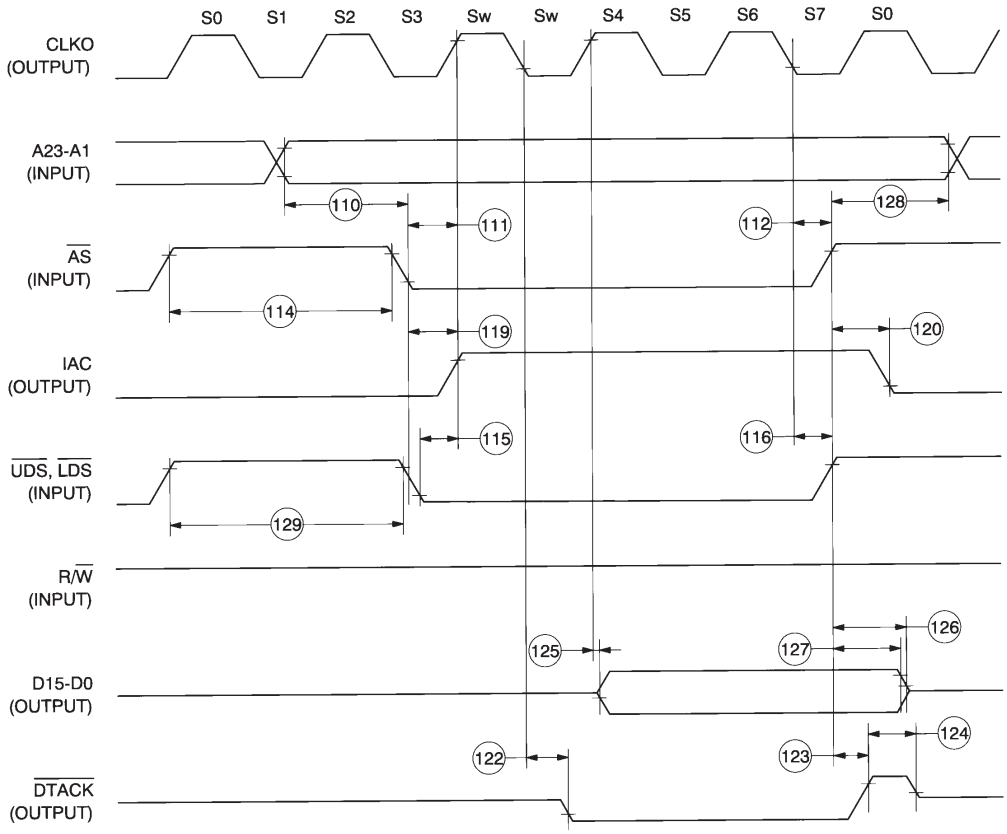


Figure 13 : External master internal synchronous read cycle timing diagram (one wait state).

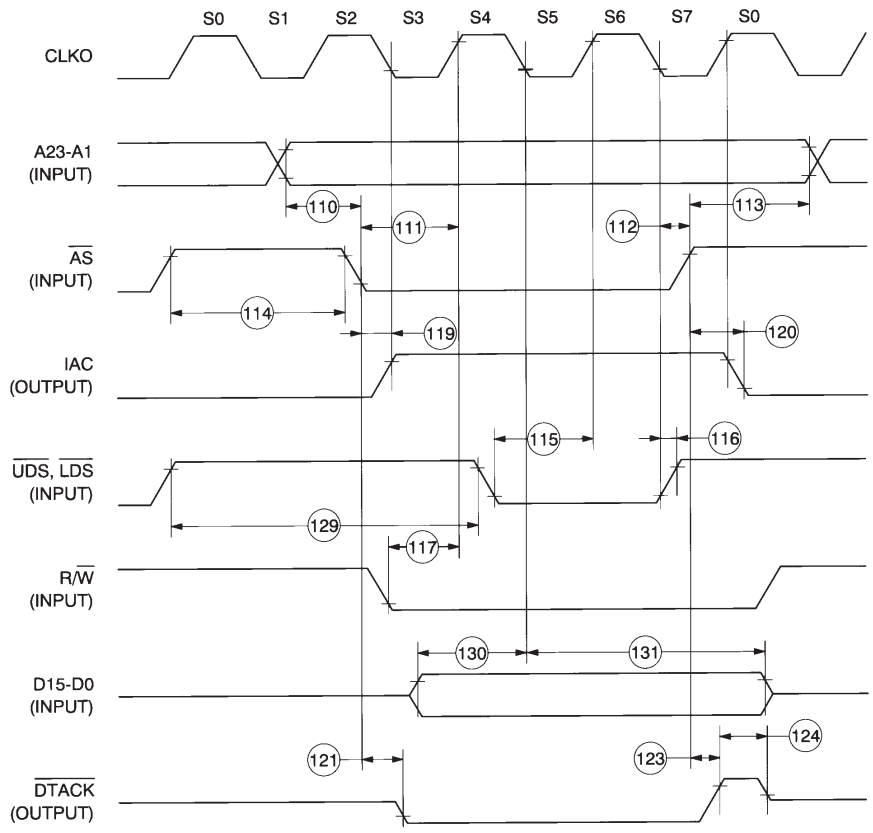


Figure 14 : External master internal synchronous write cycle timing diagram.

Table 12 · AC electrical specifications · Internal master read/write cycles (see Figure 15) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
140	t_{CHIAH}	Clock high to IAC high		40	ns
141	t_{CLIAL}	Clock low to IAC low		40	ns
142	t_{CHDTL}	Clock high to $\overline{DTACK}$ low (0 wait state)		45	ns
143	t_{CLDTH}	Clock low to $\overline{DTACK}$ high		40	ns
144	t_{CHDOV}	Clock high to data out valid		30	ns
145	t_{ASHDOH}	$\overline{AS}$ high to data out hold time	0		ns

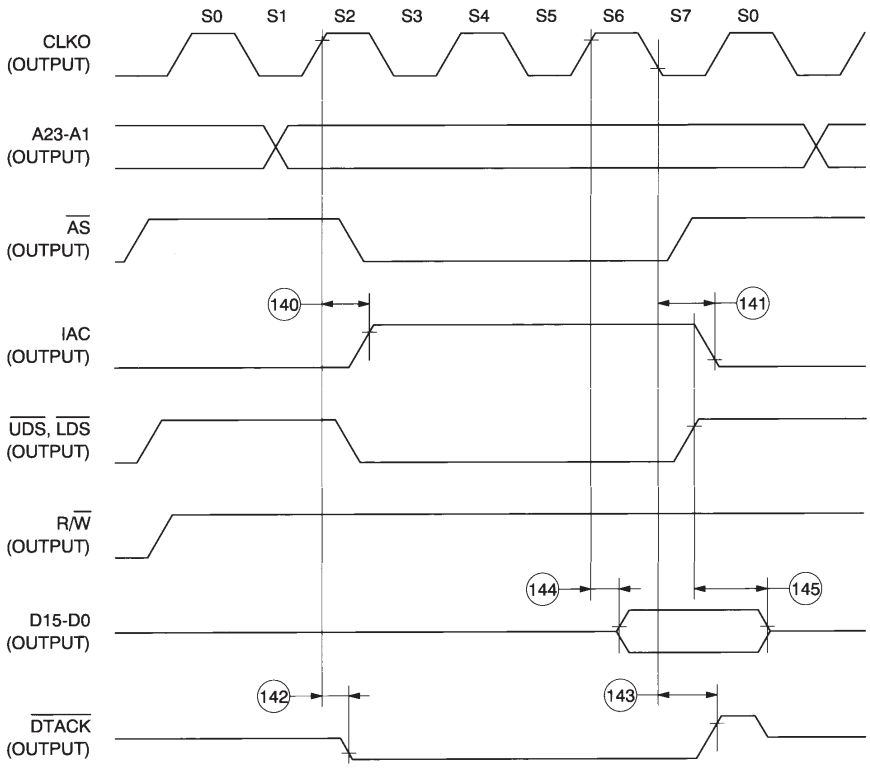


Figure 15 : Internal master internal read cycle timing diagram.

Table 13 · AC electrical specifications · Chip-select timing internal master (see Figure 16) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
150	$t_{CHCSIAKL}$	Clock high to $\overline{CS}$, $\overline{IACK}$ low - Note 1		40	ns
151	$t_{CLCSIAKH}$	Clock low to $\overline{CS}$, $\overline{IACK}$ high - Note 1		40	ns
152	t_{CSH}	$\overline{CS}$ width negated	60		ns
153	t_{CHDTKL}	Clock high to $\overline{DTACK}$ low (0 wait state)		45	ns
154	t_{CLDTKL}	Clock low to $\overline{DTACK}$ low (1-6 wait states)		30	ns
155	t_{CLDTKH}	Clock low to $\overline{DTACK}$ high		40	ns
156	t_{CHBERL}	Clock high to $\overline{BERR}$ low - Note 2		40	ns
157	t_{CLBERH}	Clock low to $\overline{BERR}$ high impedance - Note 2		40	ns
158	$t_{DTKHDTKZ}$	$\overline{DTACK}$ high to $\overline{DTACK}$ high impedance		15	ns
171	t_{IDHCL}	Input data hold time from S6 low	5		ns
172	t_{CSNDOI}	$\overline{CS}$ negated to data out invalid (write) - Note 3	10		ns
173	t_{AFVCSA}	Address, FC valid to $\overline{CS}$ asserted - Note 3	15		ns
174	t_{CSNAFI}	$\overline{CS}$ negated to address, FC invalid - Note 3	15		ns
175	t_{CSLT}	$\overline{CS}$ low time (0 wait states) - Note 3	120		ns
176	t_{CSNRWI}	$\overline{CS}$ negated to R/$\overline{W}$ invalid - Note 3	10		ns
177	t_{CSARWL}	$\overline{CS}$ asserted to R/$\overline{W}$ low (write) - Note 3		10	ns
178	t_{CSNDII}	$\overline{CS}$ Negated to data in invalid (hold time on read) - Note 3	0		ns

Note 1 : For loading capacitance less than or equal to 50 pF, subtract 4 ns from the maximum value given.
Note 2 : This specification is valid only when the ADCE or WPVE bits in the SCR are set.
Note 3 : Specs 172-178 do not have diagrams. However, similar diagrams for AS are shown as 25-11-13-14-17-20A and 29.

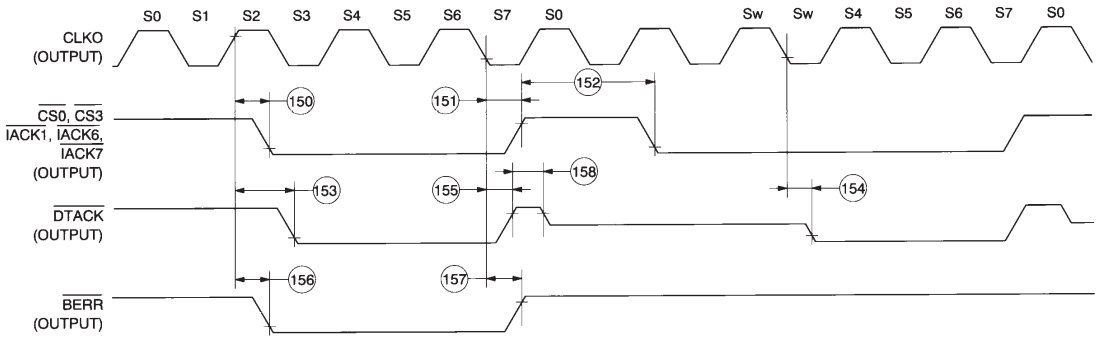


Figure 16 : Internal master chip-select timing diagram.

Table 14 - AC electrical specifications - Chip-select timing external master (see Figure 17) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
154	t_{CLDTKL}	Clock low to DTACK low (1-6 wait states)		30	ns
160	t_{ASLCSL}	AS low to CS low		30	ns
161	t_{ASHCSH}	AS high to CS high		30	ns
162	t_{AVASL}	Address valid to AS low	15		ns
163	t_{RWVASL}	R/W valid to AS low - Note 1	15		ns
164	t_{ASHAI}	AS negated to Address hold time	0		ns
165	$t_{ASLDTKL}$	AS low to DTACK low (0 wait state)		45	ns
167	$t_{ASHDTKH}$	AS high to DTACK high		30	ns
168	$t_{ASLBERL}$	AS low to BERR low - Note 2		30	ns
169	$t_{ASHBERH}$	AS high to BERR high - Notes 2 and 3		30	ns

Note 1 : The minimum value must be met to guarantee write protection operation.
Note 2 : This specification is valid when the DCE or WPVE bits in the SCR are set.
Note 3 : Also applies after a timeout of the hardware watchdog.

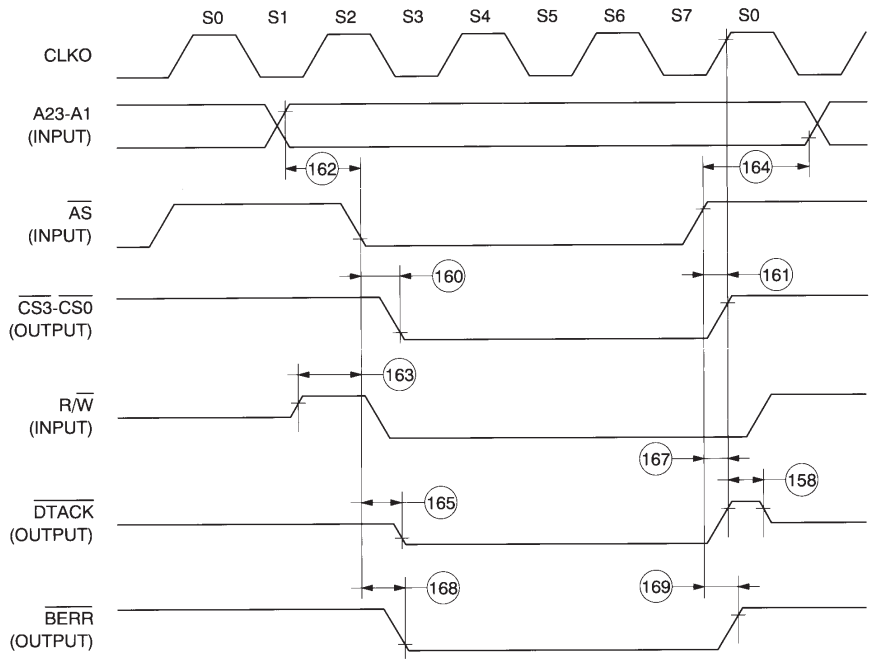


Figure 17 : External master chip-select timing diagram.

Table 15 - AC electrical specifications - Parallel I/O (see Figure 18) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
180	t_{DSU}	Input data setup time (to clock low)	20		ns
181	t_{DH}	Input data hold time (from clock low)	10		ns
182	t_{CHDOV}	Clock high to data out valid (CPU writes data, control, or direction)		35	ns

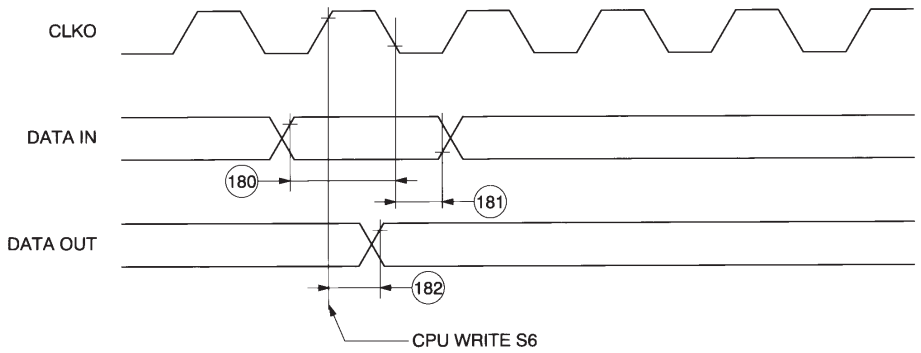


Figure 18 : Parallel I/O data in/data out timing diagram.

Table 16 - AC electrical specifications - Interrupts (see Figure 19) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Unit
190	t_{IPW}	Interrupt pulse width low $\overline{IRQ}$ (edge triggered mode)	50	ns
191	t_{AEMT}	Minimum time between active edges	3	clk
Note : Set up time for the asynchronous inputs IPL2-IPL0 and $\overline{AVEC}$ guarantees their recognition at the next falling edge of the clock.				

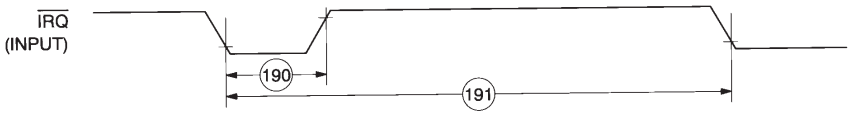


Figure 19 : Interrupts timing diagram.

Table 17 - AC electrical specifications - Timers (see Figure 20) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
200	t_{TPW}	Timer input capture pulse width	50		ns
201	t_{TICLT}	TIN clock low pulse width	50		ns
202	t_{TICHT}	TIN clock high pulse width	2		clk
203	t_{cyc}	TIN clock cycle time	3		clk
204	t_{CHTOV}	Clock high to TOUT valid		35	ns
205	t_{FRZSU}	$\overline{FRZ}$ input setup time (to clock high) - see Note	20		ns
206	t_{FRZHT}	$\overline{FRZ}$ input hold time (from clock high)	10		ns
Note : FRZ should be negated during total system reset.					

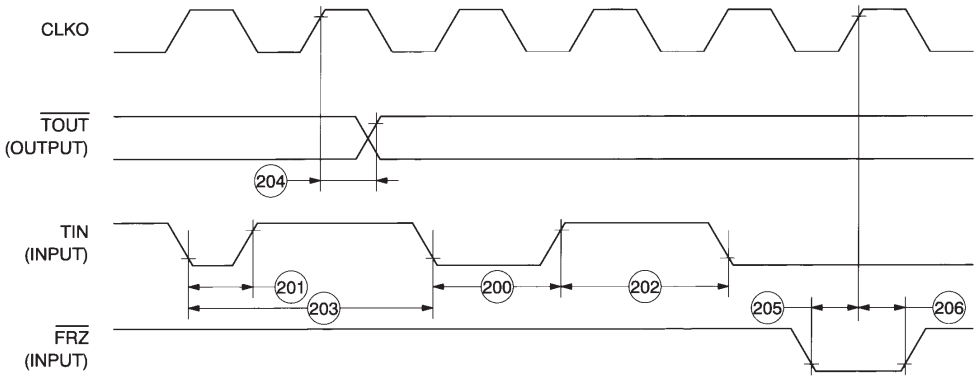


Figure 20 : Timers timing diagram.

Table 18 - AC electrical specifications - Serial communication port (see Figure 21) f = 16.67 MHz

Num.	Parameter	Min	Max	Unit
250	SPCLK clock output period	4	64	clks
251	SPCLK clock output rise/fall time		15	ns
252	Delay from SPCLK to transmit - see Note	0	40	ns
253	SCP receive setup time - see Note	40		ns
254	SPC receive hold time - see Note	10		ns
Note : This also applies when SPCLK is inverted by CI in the SPMODE register. The enable signals for the slaves may be implemented by the parallel I/O pins.				

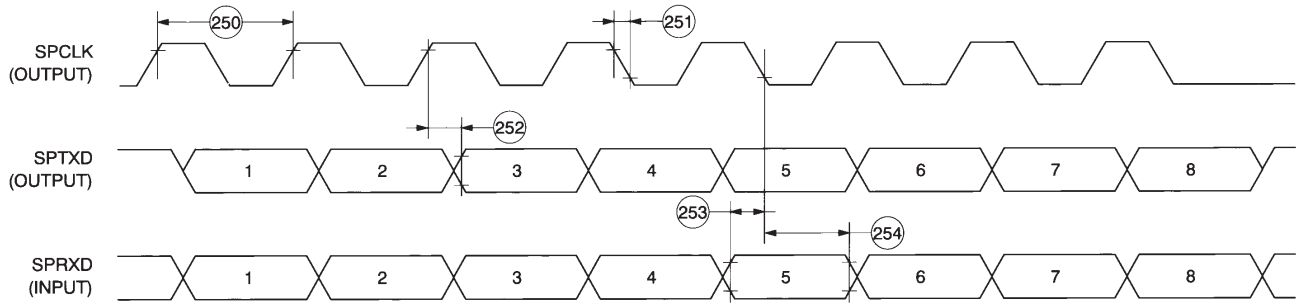


Figure 21 : Serial communication port timing diagram.

Table 19 - AC electrical specifications - IDL timing (see Figure 22) f = 16.67 MHz
All timing measurements, unless otherwise specified, are referenced to the L1CLK at 50 % point of V_{DD}

Num.	Parameter	Min	Max	Unit
260	L1CLK (IDL clock) frequency - Note 1		6.66	MHz
261	L1CLK width low	55		ns
262	L1CLK width high	60		ns
263	L1TXD, L1RQ, SDS1-SDS2 rising/falling time		20	ns
264	L1SY1 (sync) setup time (to L1CLK falling edge)	30		ns
265	L1SY1 (sync) hold time (to L1CLK falling edge)	50		ns
266	L1SY1 (sync) inactive before 4th L1CLK	0		ns
267	L1T x D active delay (from L1CLK rising edge)	0	75	ns

Table 19 - AC electrical specifications - IDL timing (continued) (see Figure 22) f = 16.67 MHz
All timing measurements, unless otherwise specified, are referenced to the L1CLK at 50 % point of V_{DD}

Num.	Parameter	Min	Max	Unit
268	L1T x D to high impedance (from L1CLK rising edge) - Note 2	0	50	ns
269	L1R x D setup time (to L1CLK falling edge)	50		ns
270	L1R x D hold time (from L1CLK falling edge)	50		ns
271	Time between successive IDL syncs	20		L1CLK
272	L1RQ valid before falling edge of L1SY1	1		L1CLK
273	L1GR setup time (to L1SY1 falling edge)	50		ns
274	L1GR hold time (from L1SY1) falling edge)	50		ns
275	SDS1-SDS2 active delay from L1CLK rising edge	10	75	ns
276	SDS1-SDS2 inactive delay from L1CLK falling edge	10	75	ns

Note 1 : The ratio CLK/L1CLK must be greater than 2.5/1.
Note 2 : High impedance is measured at the 30 % and 70 % of V_{DD} points, with the line at $V_{DD}/2$ through 10 K in parallel with 130 pF.

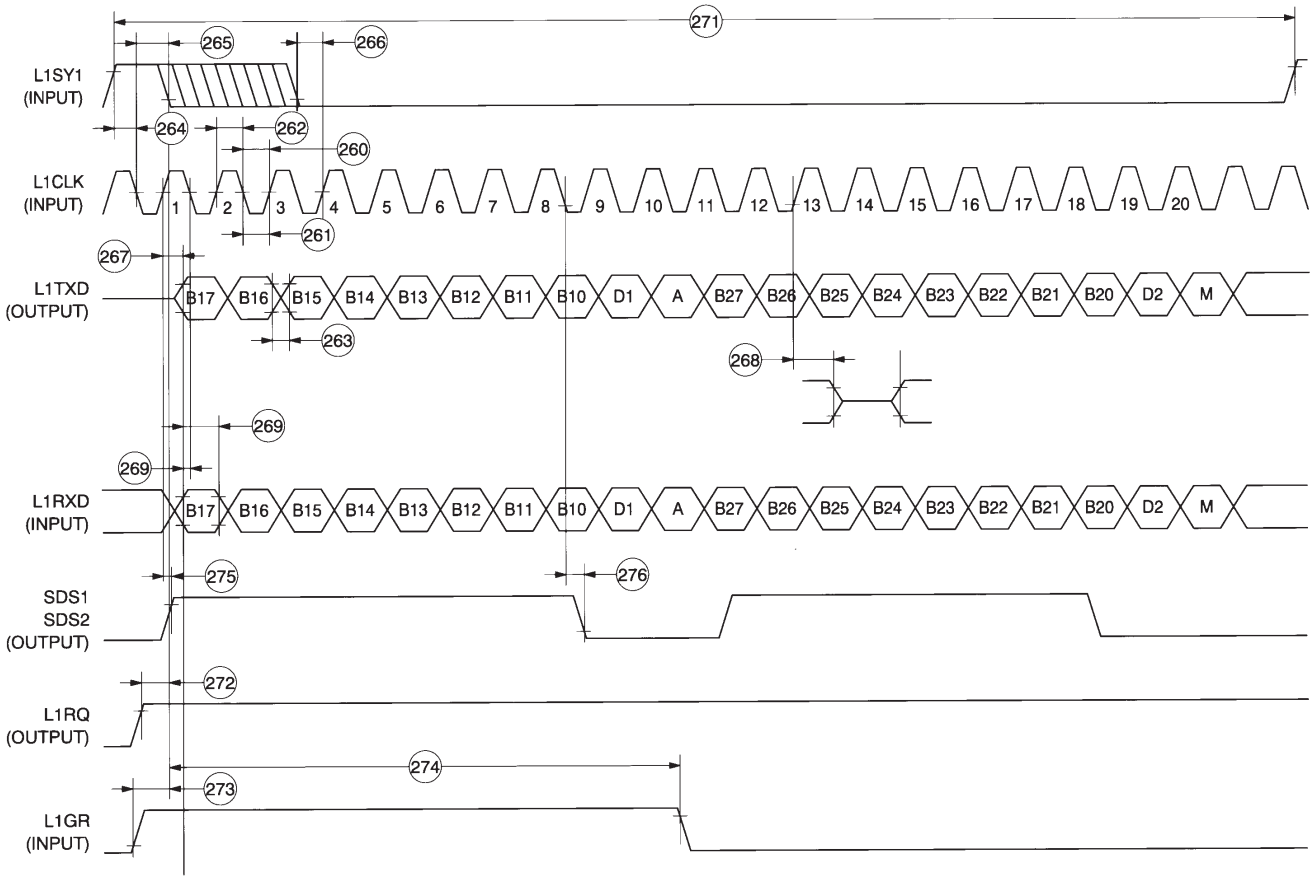


Figure 22 : IDL timing diagram.

Table 20 · AC electrical specifications · GCI timing (see Figure 23) f = 16.67 MHz

GCI supports the NORMAL mode and the GCI channel 0 (GCN0) in MUX mode.
Normal mode uses 512 kHz clock rate (256 K bit rate).
MUX mode uses 256 × n - 3088 Kbits/sec (clock rate is data rate × 2).
The ratio CLK/L1CLK must be greater than 2.5/1.

Num.	Parameter	Min	Max	Unit
	L1CLK GCI clock frequency (normal mode) - Note 1		512	kHz
280	L1CLK clock period normal mode - Note 1	1800	2100	ns
281	L1CLK width low/high normal mode	840	1450	ns
282	L1CLK rise/fall time mormal mode - Note 2	—	—	ns
	L1CLK (GCI clock) period (MUX mode) - Note 1		6.668	MHz
280	L1CLK clock period MUX mode - Note 1	150		ns
281	L1CLK width low/high MUX mode	55		ns
282	L1CLK rise/fall time MUX mode - Note 2	—	—	ns
283	L1SY1 sync setup time to L1CLK falling edge	30		ns
284	L1SY1 sync hold time from L1CLK falling edge	50		ns
285	L1T × D active delay (from L1CLK rising edge) - Note 3	0	100	ns
286	L1T × D active delay (from L1SY1 rising edge) - Note 3	0	100	ns
287	L1R × D setup time to L1CLK rising edge	20		ns
288	L1R × D hold time from L1CLK rising edge	50		ns
289	Time between successive L1SY1 in normal mode SCIT mode	64 192		L1CLK L1CLK
290	SDS1-SDS2 active delay from L1CLK rising edge - Note 4	10	90	ns
291	SDS1-SDS2 active delay from L1SY1 rising edge - Note 4	10	90	ns
292	SDS1-SDS2 inactive delay from L1CLK falling edge	10	90	ns
293	GCIDCL (GCI Data clock) active delay	0	50	ns

Note 1 : The ratio CLK/L1CLK must be greater than 2.5/1.
Note 2 : Schmitt trigger used on input buffer.
Note 3 : Condition C_L = 150 pF. L1T × D becomes valid after the L1CLK rising edge or L1SY1, whichever is later.
Note 4 : SDS1-SDS2 become valid after the L1CLK rising edge or L1SY1, whichever is later.

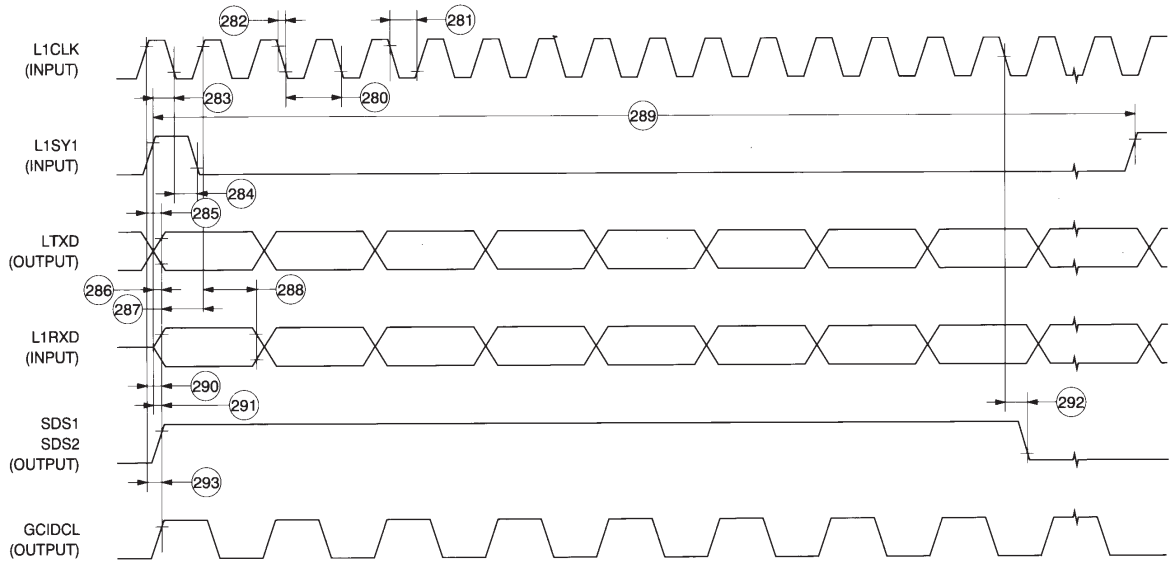


Figure 23 : GSI timing diagram.

Table 21 - AC electrical specifications - PCM timing (see Figure 24) f = 16.67 MHz

There are two syncs types :
Short frame - Sync signals are one clock cycle prior to the data.
Long frame - Sync signals are N-bits that envelope the data, N > 0.

Num.	Parameter	Min	Max	Unit
300	L1CLK (PCM clock) frequency - Note 1		6.66	MHz
301	L1CLK width low/high	55		ns
302	L1SY0-L1SY1 setup time to L1CLK falling edge	20		ns
303	L1SY0-L1SY1 hold time from L1CLK falling edge	40		ns
304	L1SY0-L1SY1 width low	1		L1CLK
305	Time between successive sync signals (short frame)	8		L1CLK
306	L1T x D data valid after L1CLK rising edge - Note 2	0	70	ns
307	L1T x D to high impedance (from L1CLK rising edge)	0	50	ns
308	L1R x D setup time (to L1CLK falling edge) - Note 3	20		ns
309	L1R x D hold time (from L1CLK falling edge) - Note 3	50		ns
310	L1T x D data valid after syncs rising edge (long) - Note 2	0	100	ns
311	L1T x D to high impedance (from L1SY0-L1SY1 falling edge) (long)	0	70	ns

Note 1 : The ratio CLK/TCLK1 must be greater than 2.5/1.
Note 2 : L1T x D becomes valid after the L1CLK rising edge or the sync enable, whichever is later, if long frames are used.
Note 3 : Specification valid for both sync methods.

Table 22 - AC electrical specifications - NMSI timing (see Figure 25)

The NMSI mode uses two clockss, one for receive and one for transmit. Both clocks can be internal or external. When the clock is internal, it is generated by the internal baud rate generator and it is output on L1RXD or L1TXD. All the timing is related to the external clock pin. The timing is specified for NMSI1. It is also valid for NMS12 and NMS13.

Num.	Parameter	Internal clock		External clock		Unit
		Min	Max	Min	Max	
315	RCLK1 and TCLK1 frequency - Note 1		5.12		6.668	MHz
316	RCLK1 and TCLK1 low/high	70		55		ns
317	RCLK1 and TCLK1 rise/fall time - Note 2	—	—	—	—	ns
318	T x D1 active delay from TCLK1 falling edge	0	40	0	70	ns
319	RTS1 active/inactive delay from TCLK1 falling edge	0	40	0	100	ns
320	CTS1 setup time to TCLK1 rising edge	50		10		ns
321	RXD1 setup time to RCLK1 rising edge	50		10		ns
322	RXD1 hold time from RCLK1 rising edge - Note 3	10		50		ns
323	CD1 setup time to RCLK1 rising edge	50		10		ns

Note 1 : The ratio CLK/TCLK1 and CLK/RCLK1 must be greater than 2.5/1 for external clock.
For internal clock the ratio must be greater than 3/1 (the input clock to the baud rate generator may be either CLK or TIM1), in both cases the maximum frequency is limited to 16.67 MHz.
In asynchronous mode (UART), the bit rate is 1/16 of the clock rate.
Note 2 : Schmitt triggers used on input buffers.
Note 3 : Also applies to $\overline{CD}$ hold time when $\overline{CD}$ is used as an external sync in BISYNC or totally transparent mode.

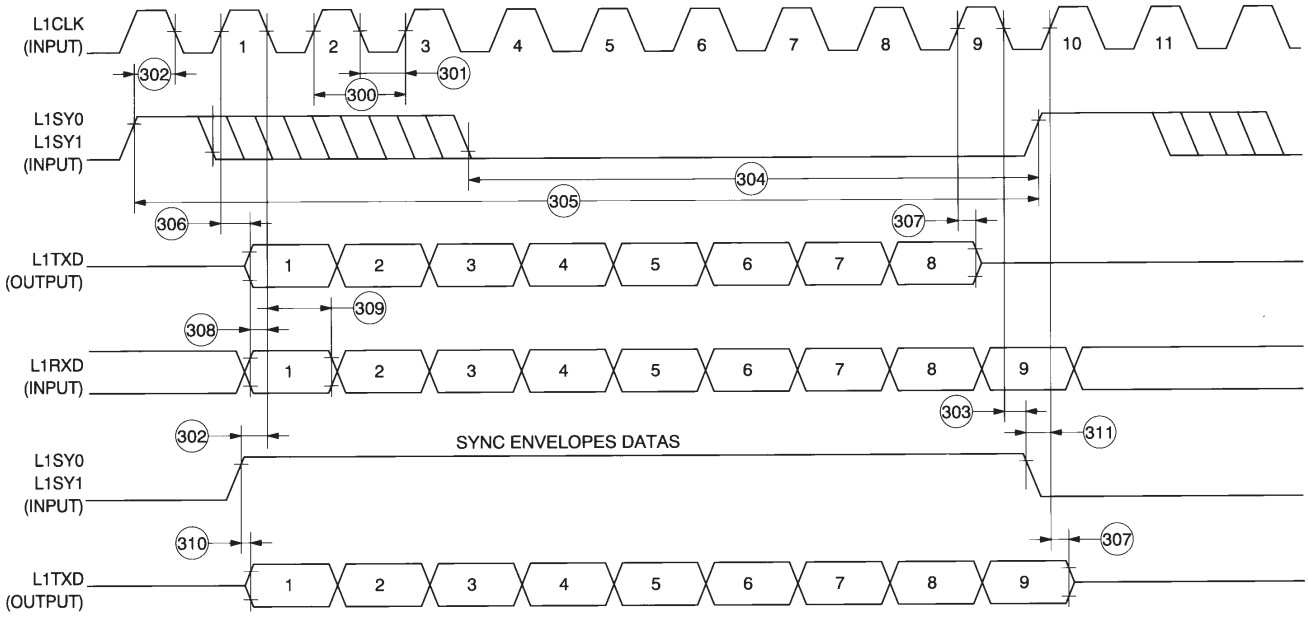


Figure 24 : PCM timing diagram.

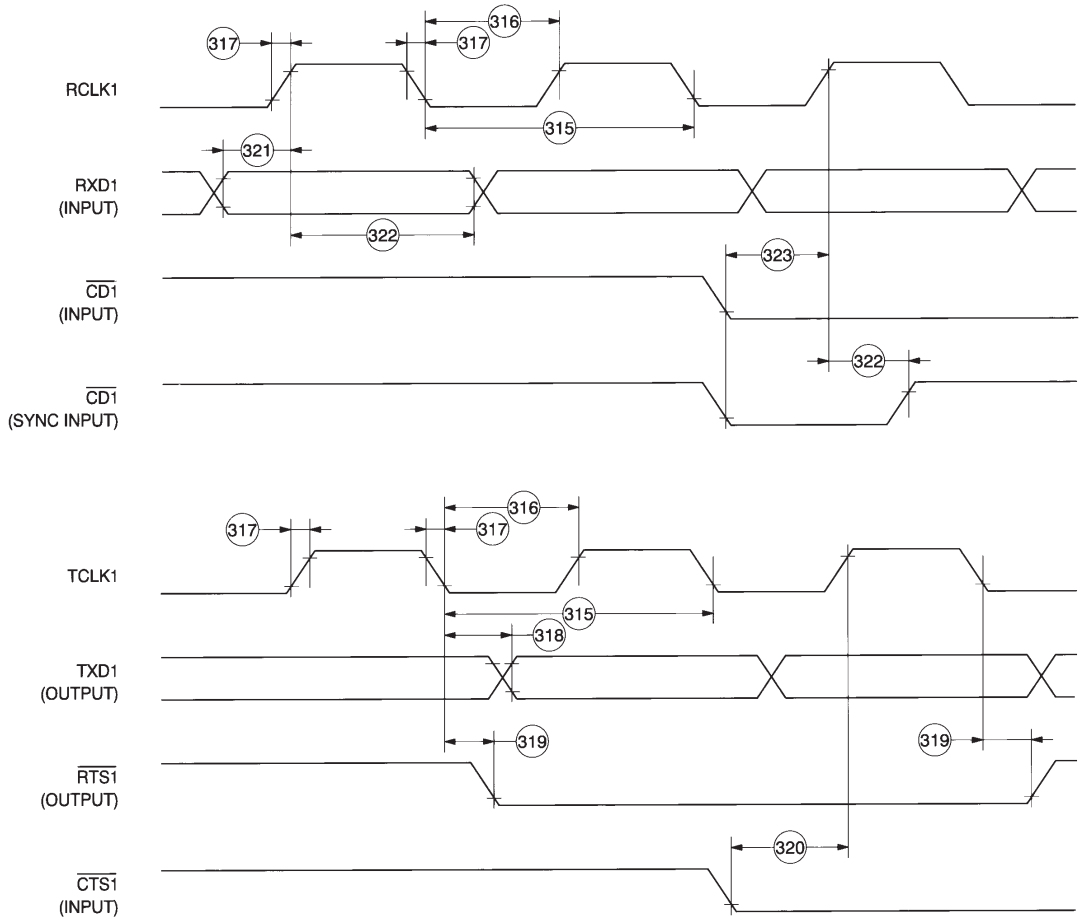


Figure 25 : NMSI timing diagram.

6 · FUNCTIONAL DESCRIPTION

The TS 68302 uses a microprocessor architecture which has peripheral devices connected to the system bus through a dual-port memory. Various parameters, counters, and all memory buffer descriptor tables reside in the dual-port RAM. The receive and transmit data buffers may be located in this on-chip RAM or in the off-chip system RAM (see Figure 26). Six DMA channels are dedicated to the six serial ports (receive and transmit for each of the three SCC channels). If an SCC channel's data is programmed to be located in the external RAM, the CP main controller (RISC processor) will program the corresponding DMA channel to perform the required accesses. If the data resides in the on-chip dual-port RAM, then the CP main controller accesses the RAM with one clock cycle access and no arbitration delays.

The buffer memory structure of the TS 68302 can be configured by software to closely match I/O channel requirements. The interrupt structure is also programmable to relieve the on-chip 68000/68008 core from bit manipulation functions for peripherals, allowing the processor to perform application software or protocol processing.

In some cases, the interface to equipment or proprietary networks may require the use of standard control and data signals. For these signals, the TS 68302 can be programmed to use the NMSI mode. This mode is available for one, two, or all three SCC ports; remaining ports may then use one of the multiplexed interface modes : IDL, GCI, or PCM.

6.1 · 68000/68008 core overview

The TS 68302 allows operation either in the full 68000 mode with a 16-bit data bus or in the 68008 mode with an 8-bit data bus.

6.2 · System integration block (SIB)

The TS 68302 has an SIB which simplifies the task of hardware and software design. The IDMA controller eliminates the need for an external DMA controller on the system board. In addition, there is an interrupt controller that can be used in a dedicated mode to generate interrupt acknowledge signals without external logic. Similarly, the chip-select signals and wait-state logic eliminate the need to generate these signals externally.

The SIB includes the IDMA controller, interrupt controller, parallel I/O ports, dual-port RAM, three timers, chip-select logic, clock generator, and system control.

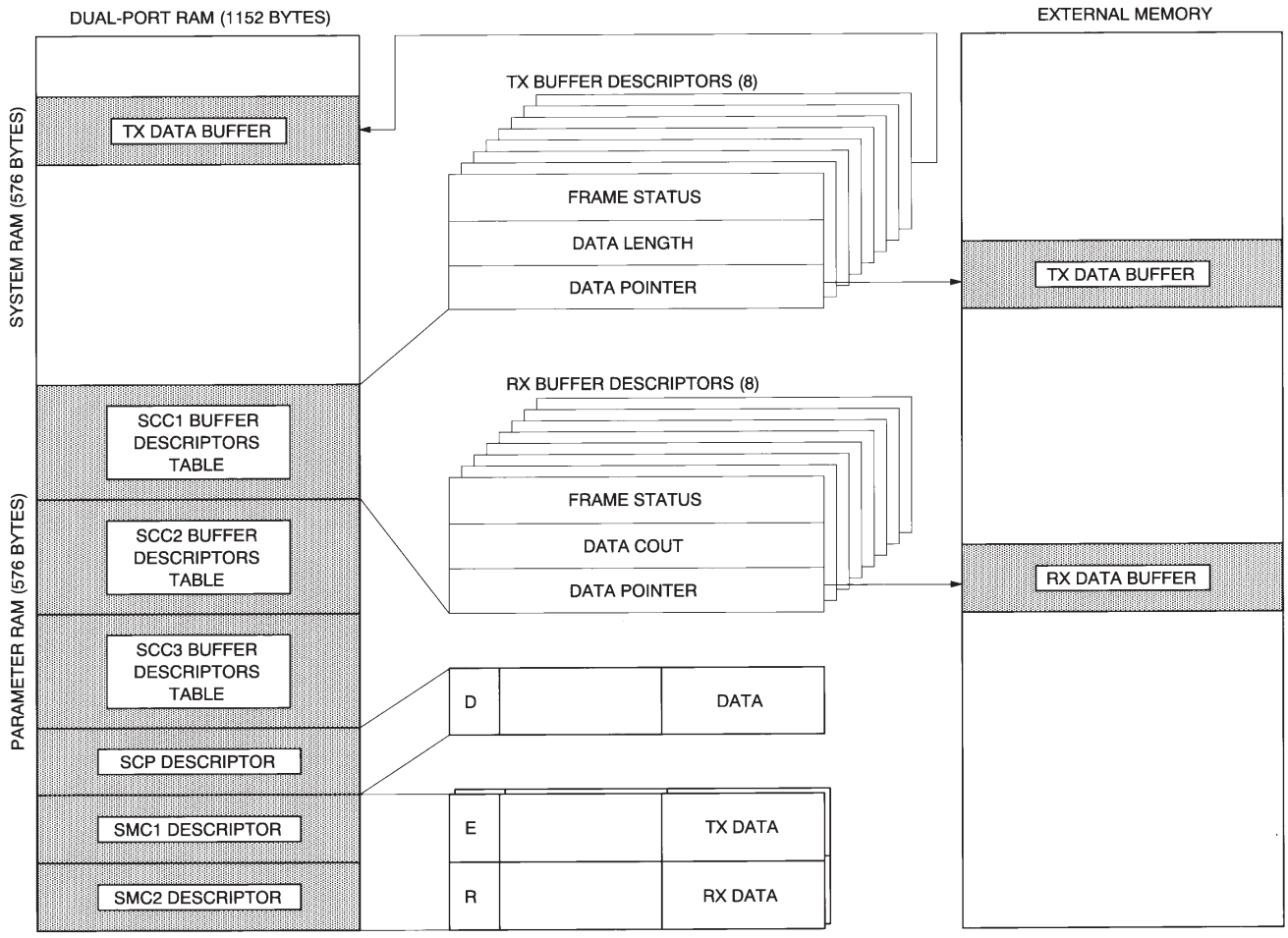


Figure 26 : Buffer memory structure.

6.2.1 - IDMA controller

The TS 68302 has one IDMA channel and six serial DMA channels which operate concurrently with other CPU operations. The IDMA can operate in different modes of data transfer as programmed by the user. The six serial DMA channels for the three full-duplex SCC channels are transparent to the user, implementing bus-cycle-stealing data transfers controlled by the TS 68302's internal RISC controller. These six channels have priority over the separate IDMA channel.

The IDMA controller can transfer data between any combination of memory and I/O devices. In addition, data may be transferred in either byte or word quantities, and the source and destination addresses may be either odd or even. Every IDMA cycle requires between two and four bus cycles, depending on the address boundary and transfer size. If both the source and destination addresses are even, the IDMA fetches one word of data and then immediately deposits it. If either the source or destination block begins on an odd boundary, the transfer takes more bus cycles.

The IDMA features are as follows :

- memory-memory, memory-peripheral, or peripheral-memory data transfers,
- operation with data blocks located at even or odd addresses,
- packing and unpacking of operands,
- fast transfer rates : up to 4 MBps at 16 MHz with no wait states,
- full support of all bus exceptions : halt, bus error, and retry,
- flexible request generation
- two address pointer registers and one counter register,
- three I/O lines for externally requested data transfers,
- asynchronous bus structure with 24-bit address and 8-/16 bit data bus.

6.2.2 - Interrupt controller

The interrupt controller, which manages the priority of internal and external interrupt requests, generates a vector number during the CPU interrupt acknowledge cycle. Nested interrupts are fully supported.

The interrupt controller receives requests from internal sources (INRQ interrupts) such as the timers, the IDMA, the serial controllers, and the parallel I/O pins (port B). The interrupt controller allows the masking of each INRQ interrupt source. When multiple events within a peripheral can cause the interrupt, each of these events is also maskable.

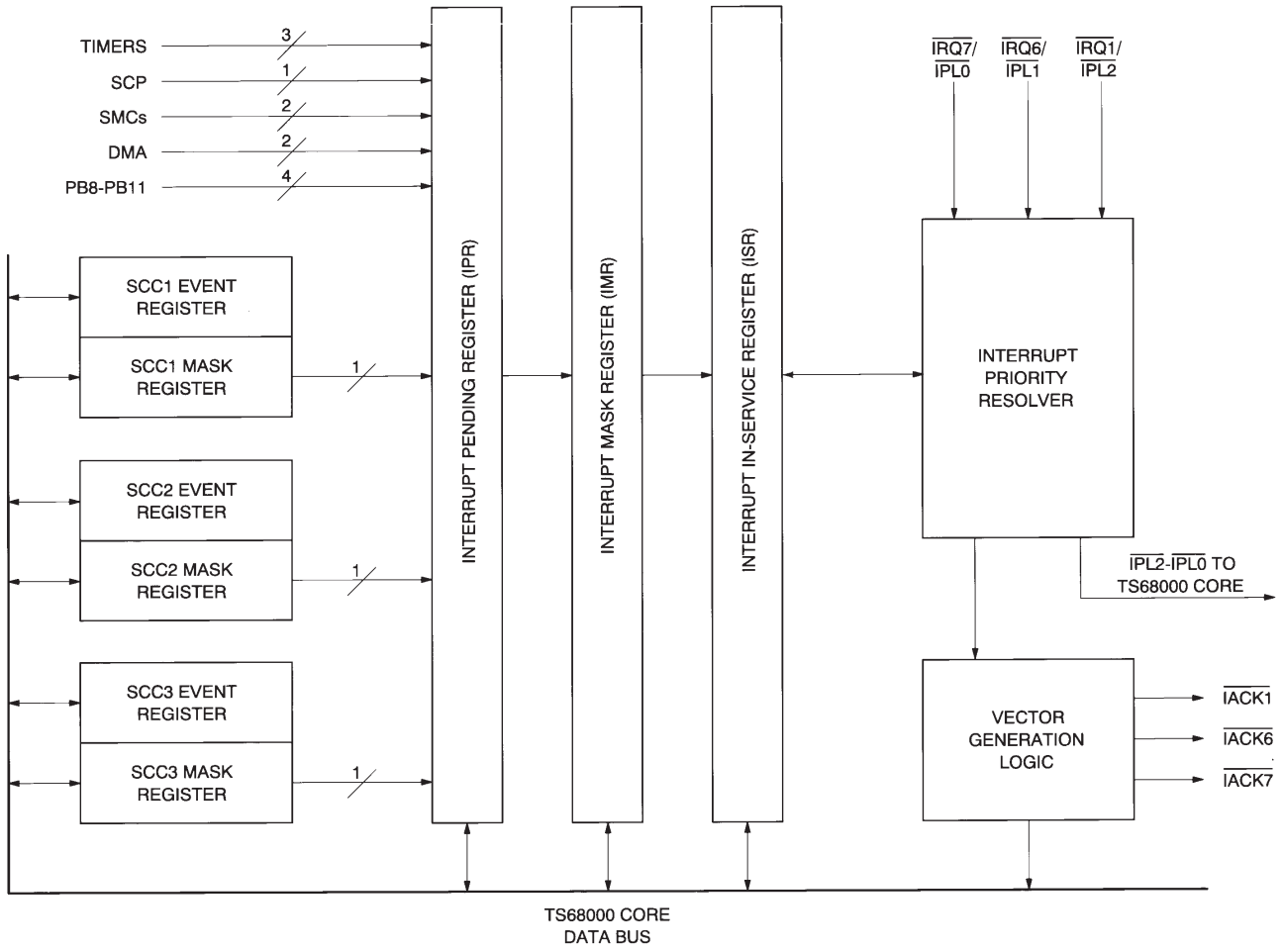


Figure 27 : Interrupt controller block diagram.

The interrupt controller also receives external (EXRQ) requests. EXRQ interrupts are received by the IMP according to the operational mode selected. In the normal operational mode, EXRQ interrupts are encoded onto the IPL lines. In the dedicated operational mode, EXRQ interrupts are presented directly as IRQ7, IRQ6, and IRQ1.

The interrupt controller block diagram is shown in Figure 27. The interrupt controller features are as follows :

- two operational modes : normal and dedicated,
- eighteen priority-organized interrupt sources (internal and external),
- fully nested interrupt environment,
- unique vector number for each internal/external source,
- three selectable interrupt request/interrupt acknowledge pairs.

6.2.3 · Parallel I/O ports

Port A and port B are two general-purpose I/O ports. Each pin in the 16-bit port A may be configured as a general-purpose I/O pin or as a dedicated peripheral interface pin. Port B has 12 pins. Eight pins may be configured as general-purpose pins or as dedicated peripheral interface pins, and four are general-purpose pins, each with interrupt capability.

6.2.4 · Dual-port RAM

The IMP has 1152 bytes of RAM configured as a dual-port memory. The RAM can be accessed by the internal RISC controller or one of three bus masters : the 68000 core, an external bus master, or the IDMA. All internal bus masters synchronously access the RAM with no wait states. External bus masters can access the RAM and registers synchronously or asynchronously.

The RAM is divided into two parts. There are 576 bytes used as a parameter RAM, which includes pointers, counters, and registers for the serial ports. The other 576 bytes may be used for system RAM, which may include data buffers, or may be used for other purposes such as a no-wait-state cache.

6.3 · Timers

There are three timer units. Two units are identical, general-purpose timers; the third unit can be used to implement a watchdog timer function.

The two general-purpose timers are implemented with a timer mode register (TMR), a timer capture register (TCR), a timer counter (TCN), a timer reference register (TRR), and a timer event register (TER). The TMR contains the prescaler value programmed by the user. The watchdog timer, which has a TRR and TCN, uses a fixed prescaler value.

The timer features are as follows :

- Two general-purpose timer units :
  - maximum period of 16 seconds (at 16.67 MHz),
  - 60-nanosecond resolution (at 16.67 MHz),
  - programmable sources for the clock input,
  - input capture capability,
  - output compare with programmable mode for the output pin,
  - free run and restart modes.
- One watchdog timer with a 16-bit counter and a reference register :
  - maximum period of 16 seconds (at 16.67 MHz),
  - 0.5-millisecond resolution (at 16 MHz),
  - output signal (WDOG),
  - interrupt capability.

6.4 · External chip-select signals and wait-state logic

The TS 68302 has a set of four programmable chip-select signals. Each chip select has an identical structure. For each memory area, an internally generated cycle-termination signal (DTACK) may be defined with up to six wait states to avoid using board space for cycle-termination logic. The four signals may each support four different classes of memory, such as high-speed static RAM, slower dynamic RAM, EPROM, and nonvolatile RAM. The chip-select and wait-state generation logic is active for all potential bus masters.

6.5 · Clock generator

The TS 68302 has an on-chip clock generator which supplies internal and external high-speed clocks (up to 16.67 MHz). The clock circuitry uses three dedicated pins : EXTAL, XTAL, and CLKO.

6.6 · System control

The IMP system control consists of a system control register (SCR) containing bits for the following system control functions :

- system status and control logic,
- bus arbitration logic with low interrupt latency,
- hardware watchdog,
- low power (standby) modes,
- disable CPU logic (68000),
- freeze control for debugging on-chip peripherals,
- AS control during read-modify-write cycles.

6.6.1 · System control register

The SCR is a 32-bit register that consists of system status and control bits, a bus arbiter control bit, hardware watchdog control bits, low power control bits, and freeze select bits. The eight most significant bits of the SCR report events recognized by the system control logic and set the corresponding bit in the SCR.

The low power modes are used, when no processing is required from the 68000/68008 core, to reduce the system power consumption to its minimum value. The low power modes may be exited by an interrupt from an on-chip peripheral.

6.6.2 · Disable CPU logic (68000)

This control allows an external processor direct connection to the bus and to the IMP's peripherals while the on-chip 68000 core is disabled. Entered during a system reset ($\overline{RESET}$ and $\overline{HALT}$ asserted together), this mode configures the IMP on-chip peripherals for use with other TS 68032 units or other processors and is an effective configuration for systems needing more than three SCCs.

6.6.3 · Freeze control

This control is used to freeze the activity of selected peripherals and to debug systems. The IMP freezes its activity with no new interrupt requests, no memory accesses (internal or external), and no access of the serial channels. The IDMA controller completes any bus cycle in progress and releases bus ownership. No further bus cycles will be started as long as $\overline{FRZ}$ remains asserted.

6.7 · DRAM refresh controller

The CP main (RISC) controller can optionally handle the dynamic RAM (DRAM) refresh task without any intervention from the 68000 core. The refresh request can be generated from an TS 68302 timer, baud rate generator, or externally. The DRAM refresh controller performs a standard 68000-type read cycle at programmable address sequences, with user-provided RAS and CAS generation.

6.8 · Communications processor

The CP in the TS 68302 includes the main controller, six serial DMA channels, three SCCs, an SCP, and two SMCs.

Host software configures each communications channel, as required by the application, to include parameters, baud rates, physical channel interfaces desired, and interrupting conditions. Buffer structures are set up for receive and transmit channels. Up to eight frames may be received or transmitted without host software involvement. Selection of the interrupt interface is also set by register bits in register space of the device.

Data is transmitted and received using the appropriate buffer descriptors and buffer data space for a given channel. The CP operates is a modified polling mode on each channel and buffer descriptor to identify buffers awaiting transmission and channels requiring servicing. The user sets a bit in the buffer descriptor of a transmit frame ; when the CP polls and detects this bit, it will begin transmission. Generally, no other action is required to accomplish transmission.

6.8.1 · Main controller

The main controller is a microcode RISC processor that services all the serial channels. The main controller transfers data between the serial channels and internal/external RAM, executes host commands, and generates interrupts to the interrupt controller.

Data is transferred from the serial channel to the dual-port RAM or to the external memory through the peripheral bus. If data is transferred between the SCC channels and external memory, the main controller uses up to six serial DMA channels for the transfer. The main controller also controls all character and address comparison and cyclic redundancy check (CRC) generation and checking.

The execution unit includes the arithmectic logic unit (ALU), which performs arithmetic and logic operations on the registers.

6.8.2 · Serial Communication Controllers

The TS 68302 has three independent SCCs. Each SCC can be configured to implement different protocols – for example, to perform a gateway function or to interface to an ISDN basic rate channel. To simplify programming, each protocol implementation uses identical data structures.

Five protocols are supported : high-level data link control (HDLC), binary synchronous communication (BISYNC), synchronous/asynchronous digital data communications message protocol (DDCMP), V.110, universal asynchronous receiver transmitter (UART), and a fully transparent mode. To aid system diagnostics, each SCC may be configured to operate in either an echo or loopback mode. In echo mode, the IMP retransmits any signals received; in loopback mode, the IMP locally receives signals originating from itself.

The clock pins (RCLK, TCLK) for each SCC can be programmed for either an external or internal source, with user-programmable baud rates available for each SCC channel.

Each SCC also supports the standard modem control signals : request to send ($\overline{RTS}$), clear to send ($\overline{CTS}$), and carrier detect ($\overline{CD}$). Other modem signals may be provided through the parallel I/O pins.

The SCC features are as follows :

- programmable baud rate generator driven by the internal or external clock,
- data may be clocked by the programmable baud rate generator or directly by an external clock,
- provides modem signals $\overline{RTS}$, $\overline{CTS}$, and $\overline{CD}$,
- Full-duplex operation,
- Automatic echo mode,

- Local loopback mode,
- Baud rate generator outputs available externally.

The SCC HDLC mode key features are as follows :

- flexible data buffers with multiple buffers per frame allowed,
- separate interrupts for frames and buffers (receive and transmit),
- four address comparison registers with mask,
- maintenance of five 16-bit error counters,
- flag/abort/idle generation/detection,
- zero insertion/deletion,
- NRZ/NRZI data encoding,
- 16-bit or 32-bit CRC-CCITT generation/checking,
- detection of non-octet aligned frames,
- detection of frames that are too long,
- programmable 0-15 FLAGS between successive frames,
- automatic retransmission in case of collision.

The SCC BISYNC mode key features are as follows :

- flexible data buffers,
- eight control character recognition registers,
- automatic SYNC1 and SYNC2 detection,
- SYNC/DLE stripping and insertion,
- CRC-16 and LRC generation/checking,
- parity (VRC) generation/checking,
- supports BISYNC transparent operation (use of DLE characters),
- supports promiscuous (totally transparent) reception and transmission,
- maintains parity error counter,
- external SYNC support,
- reverse data mode.

The SCC DDCMP mode key features are as follows :

- synchronous or asynchronous DDCMP links supported,
- flexible data buffers,
- four address comparison registers with mask,
- automatic frame synchronization,
- automatic message synchronization by searching for SOH, ENQ, or DLE,
- CRC-16 generation/checking,
- NRZ/NRZI data encoding,
- maintenance of four 16-bit error counters.

The SCC V.110 mode key features are as follows :

- provides synchronization and reception of 80-bit frames,
- automatic detection of framing errors,
- allows transmission of the 80-bit frame.

The SCC UART mode key features are as follows :

- flexible message-oriented data buffers,
- multidrop operation,
- receiver wakeup on idle line or address mode,
- eight control character comparison registers,
- two address comparison registers,
- four 16-bit error counters,

- programmable data length (7-8 bits),
- programmable 1 or 2 stop bits with fractional stop bits,
- even/odd/force/no parity generation,
- even/odd/no parity check,
- frame error, noise error, break, and idle detection,
- transmits idle and break sequences,
- freeze transmission option,
- maintenance of four 16-bit error counters,
- provides asynchronous link over which DDCMP may be used,
- Flow control character transmission supported.

6.8.3 · Serial communication port

The SCP is a full-duplex, synchronous, character-oriented channel which provides a three-wire interface (TXD, RXD, and clock). The SCP consists of independent transmitter and receiver sections and a common SCP clock generator. The transmitter and receiver section use the same clock, which is derived from the main clock by an on-chip baud rate generator. The TS 68302 is an SCP master, generating both the enable and the clock signals. The enable signals may be generated by the general-purpose I/O pins.

The SCP allows the TS 68302 to communicate with a variety of serial devices for the exchange of status and control information using a subset of the Motorola serial peripheral interface (SPI). Such devices may include industry-standard CODECs and other microcontrollers and peripherals.

The SCP can be configured to operate in a local loopback mode, which is useful for diagnostic functions. The receiver and the transmitter operate normally in these modes.

The SCP features are as follows :

- three-wire interface (SPTXD, SPRXD, and SPCLK),
- full-duplex operation,
- clock rate up to 4.096 MHz,
- programmable baud rate generator,
- local loopback capacibility for testing purposes.

6.8.4 · Serial management controllers

The SMCs are two synchronous, full-duplex ports that may be configured to operate in either IDL or GCI mode to handle the maintenance and control portions of these interfaces. The SMC ports are not used in PCM or NMSI modes. The SMC features are as follows :

- two modes of operation - IDL and GCI,
- local loopback capability for testing purposes,
- full-duplex operation,
- SMC1 in GCI mode detects collisions on the D channel.

6.8.5 · Serial channels physical interface

The serial channels physical interface connects the physical layer serial lines and the serial controllers (three SCCs and two SMCs). The interface implements both the routing and the time-division multiplexing for the full ISDN bandwidth. It supports four buses : IDL, GCI, PCM, and NMSI (a nonmultiplexed modem interface). The multiplexed modes (IDL, GCI, and PCM) also allow multiplie channels (e.g., ISDN B channels) or user-defined subchannels to be assigned to a given SCC. The serial interface also supports two testing modes : echo and loopback.

For the IDL and GCI buses, support of management functions in the frame structure is provided by the SCP or SMCs, respectively. Refer to Figure 28 for the serial channels physical interface block diagram.

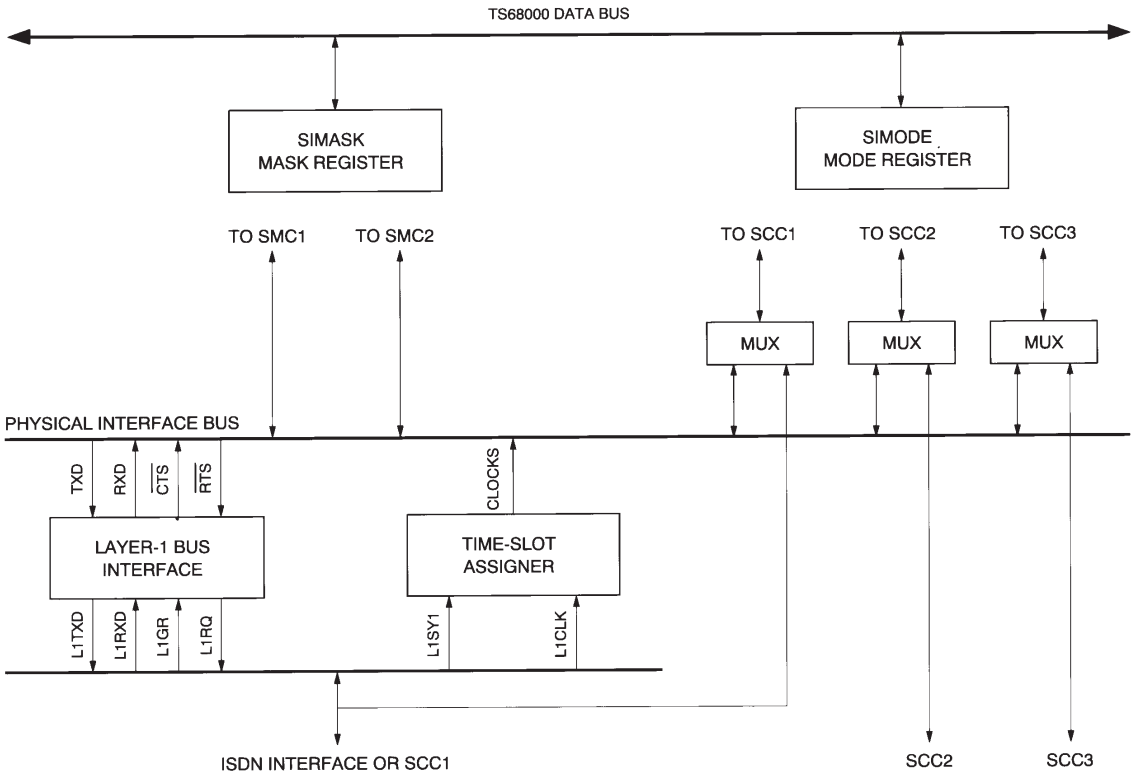


Figure 28 : Serial channels physical interface block diagram.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-STD-1835.

7.2 - Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or TCS standards and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

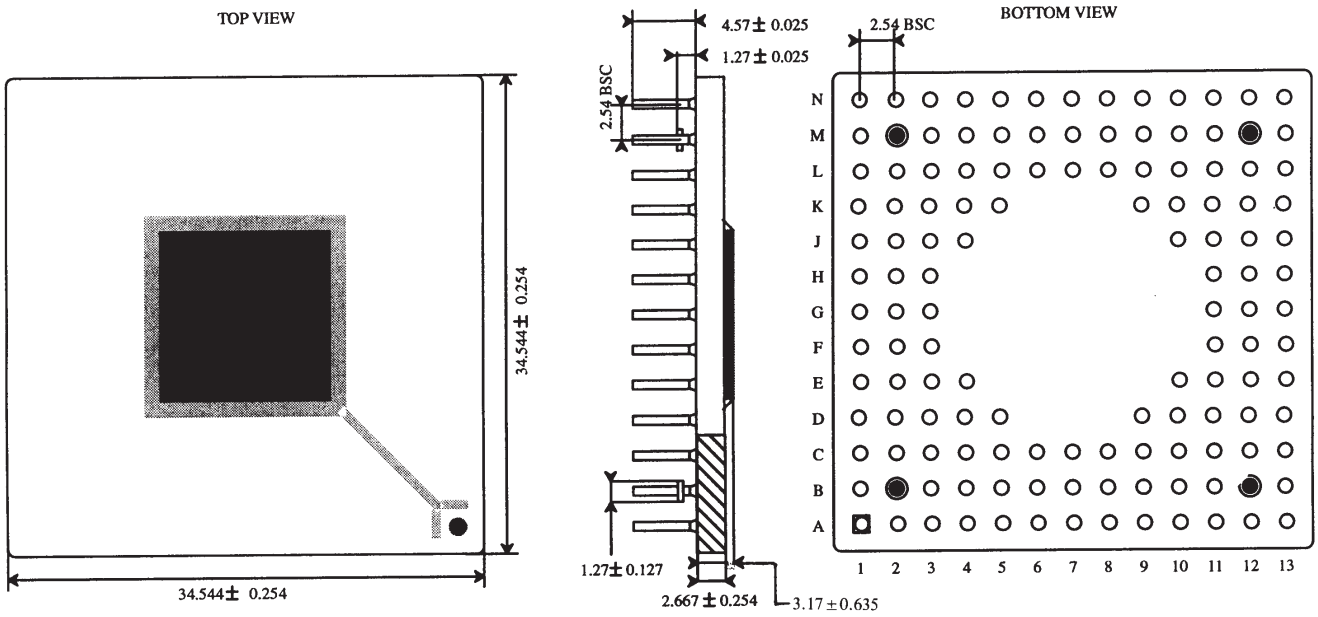
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

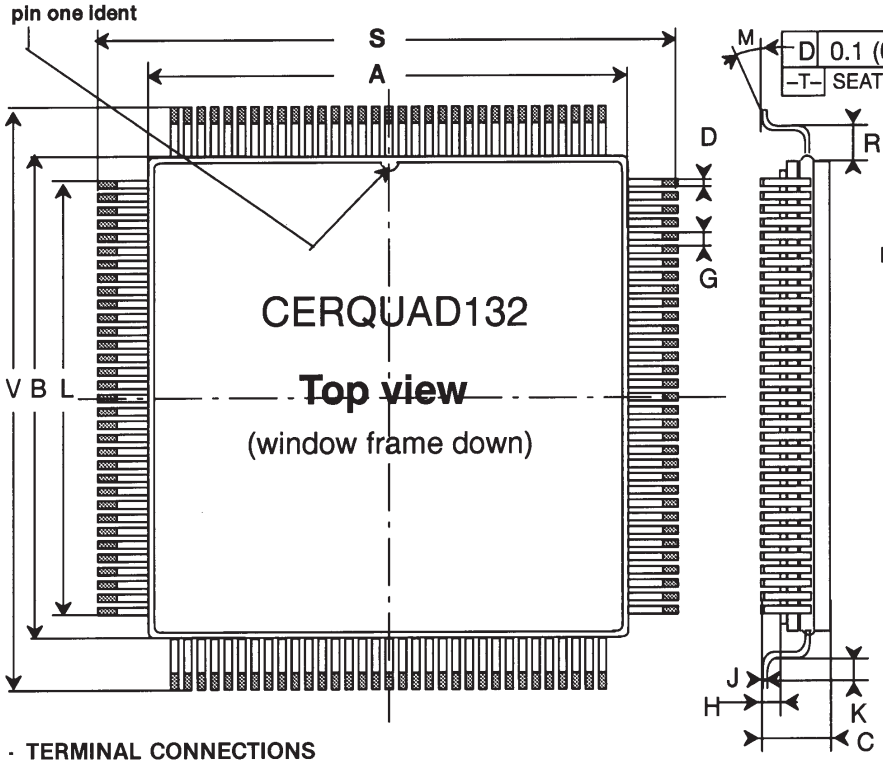
f) Maintain relative humidity above 50 %, if practical.

9 - PACKAGE MECHANICAL DATA

9.1 - 132 pins - Ceramic Pin Grid Array (in millimeter)



9.2 - 132 pins - Ceramic Quad Flat Pack / CERQUAD



	Milimeters		Inches	
DIM	MIN	MAX	MIN	MAX
A	21.85	22.86	0.86	0.90
B	21.85	22.86	0.86	0.90
C	3.94	4.52	0.155	0.178
D	0.204	0.292	0.008	0.0115
G	0 64	BSC	0.025	BSC
H	0.5	1.0	0.019	0.039
J	0.13	0.20	0.005	0.008
K	0.51	0.76	0.020	0.030
L	20.32	REF	0.800	REF
R	0.64	–	0.025	–
S	27.23	27.63	1.072	1.088
V	27.23	27.63	1.072	1.088
M	0°	8°	0°	8°

10 - TERMINAL CONNECTIONS

10.1 - 132 pins - Ceramic Pin Grid Array

See Figure 2.1 page 4.

10.2 - 132 pins - Ceramic Quad Flat Pack / CERQUAD

See Figure 2.2 page 4.

11 - ORDERING INFORMATION

11.1 - Hi-REL product

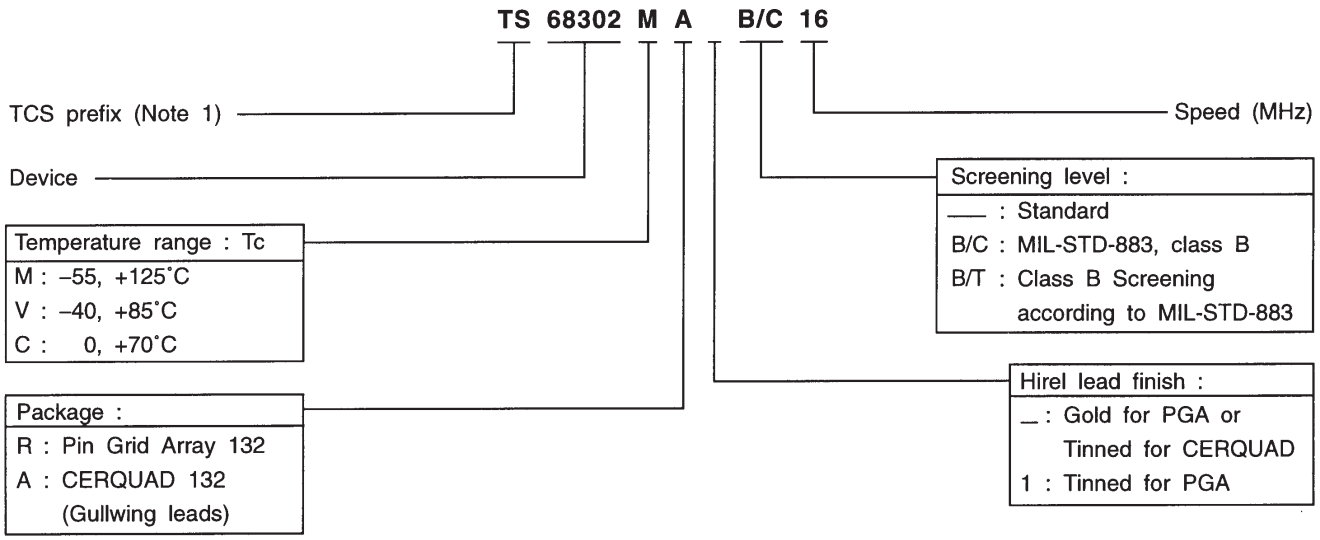
Commercial TCS Part-Number Note 1	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68302MRB/C16	MIL-STD-883	PGA 132	– 55 / + 125	16.67	–
TS68302MA7B/C16	MIL-STD-883	CERQUAD 132 Note 2	– 55 / + 125	16.67	–
TS68302DESC01XC	DESC	PGA 132	– 55 / + 125	16.67	5962-93159
TS68302DESC01YA	DESC	CERQUAD 132 Note 2	– 55 / + 125	16.67	5962-93159

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : Gullwing leads.

11.2 - Standard product

Commercial TCS Part-Number Note 1	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68302VR16	TCS Standard	PGA 132	– 40 / + 85	16.67	Internal
TS68302MR16	TCS Standard	PGA 132	– 55 / + 125	16.67	Internal
TS68302VA16	TCS Standard	CERQUAD 132 Note 2	– 40 / + 85	16.67	Internal
TS68302MA16	TCS Standard	CERQUAD 132 Note 2	– 55 / + 125	16.67	Internal

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : Gullwing leads.


TS 68302 M A B/C 16
TCS prefix (Note 1)
Device
Speed (MHz)
Screening level :
— : Standard
B/C : MIL-STD-883, class B
B/T : Class B Screening according to MIL-STD-883
Temperature range : Tc
M : –55, +125°C
V : –40, +85°C
C : 0, +70°C
Hirel lead finish :
_ : Gold for PGA or Tinned for CERQUAD
1 : Tinned for PGA
Package :
R : Pin Grid Array 132
A : CERQUAD 132 (Gullwing leads)

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